

Model Name : Stonic_RNS
Compal Project Name : FH51S
File Name : LA-K181P

Compal Confidential

FH51S MB Schematics Document

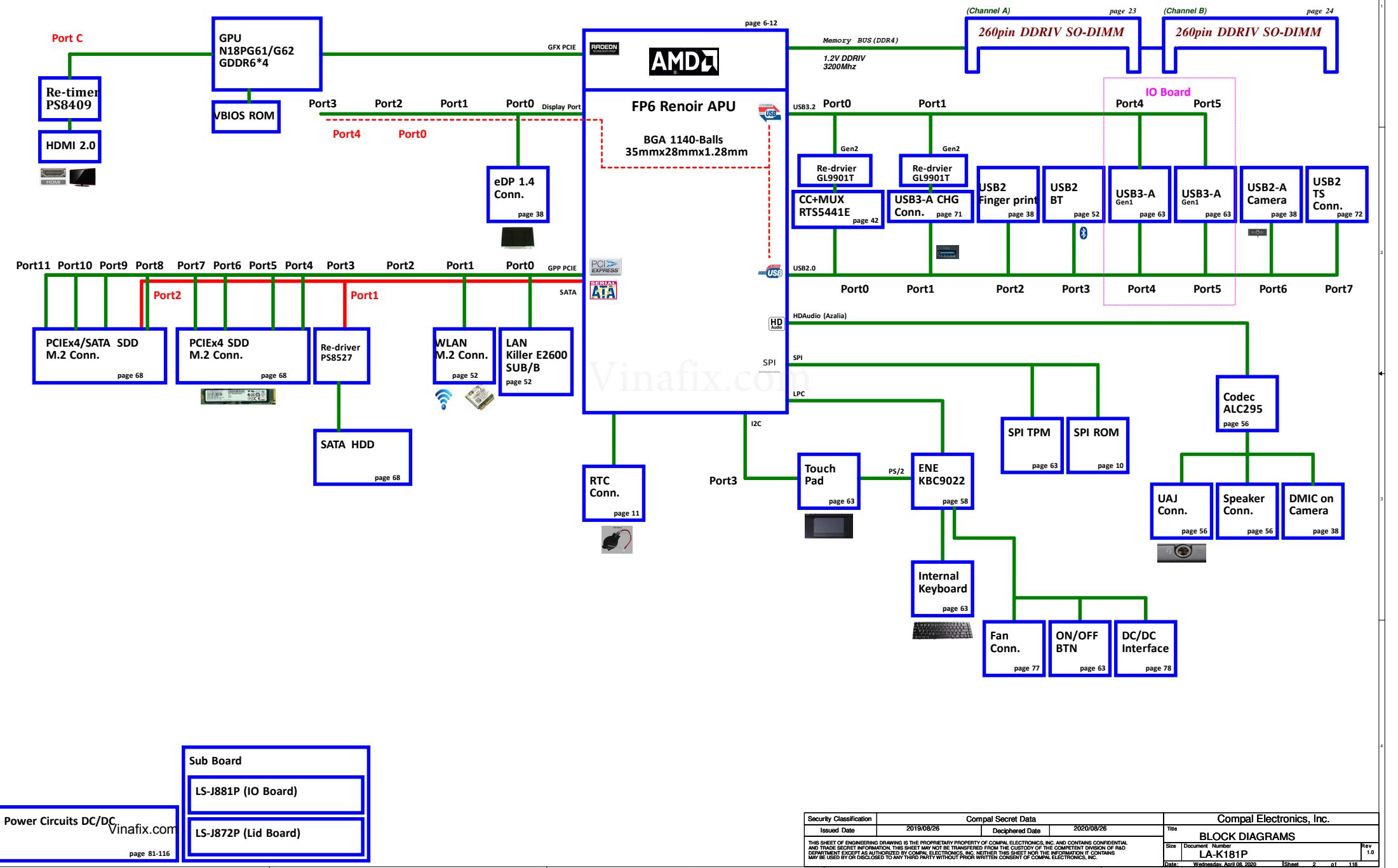
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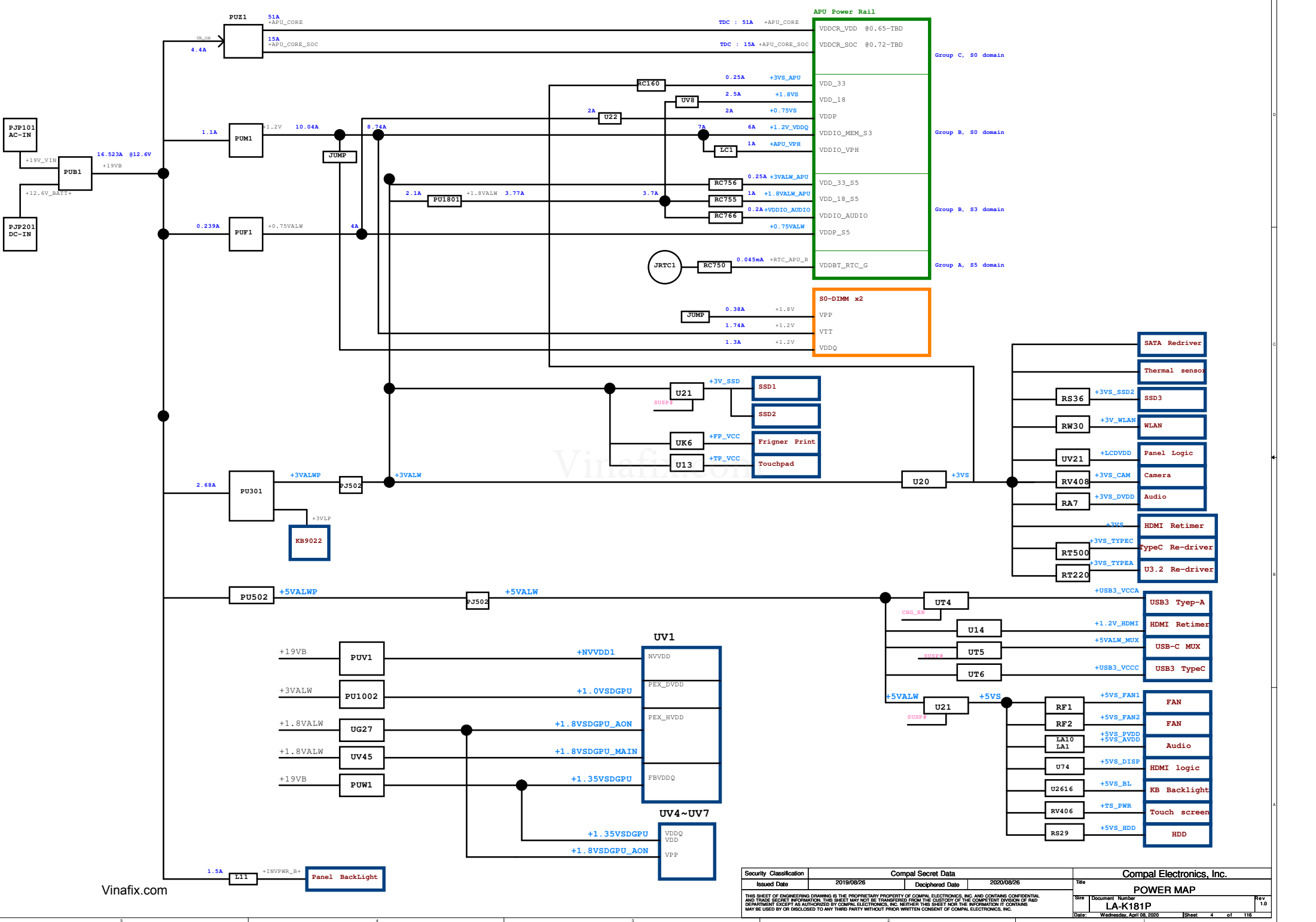
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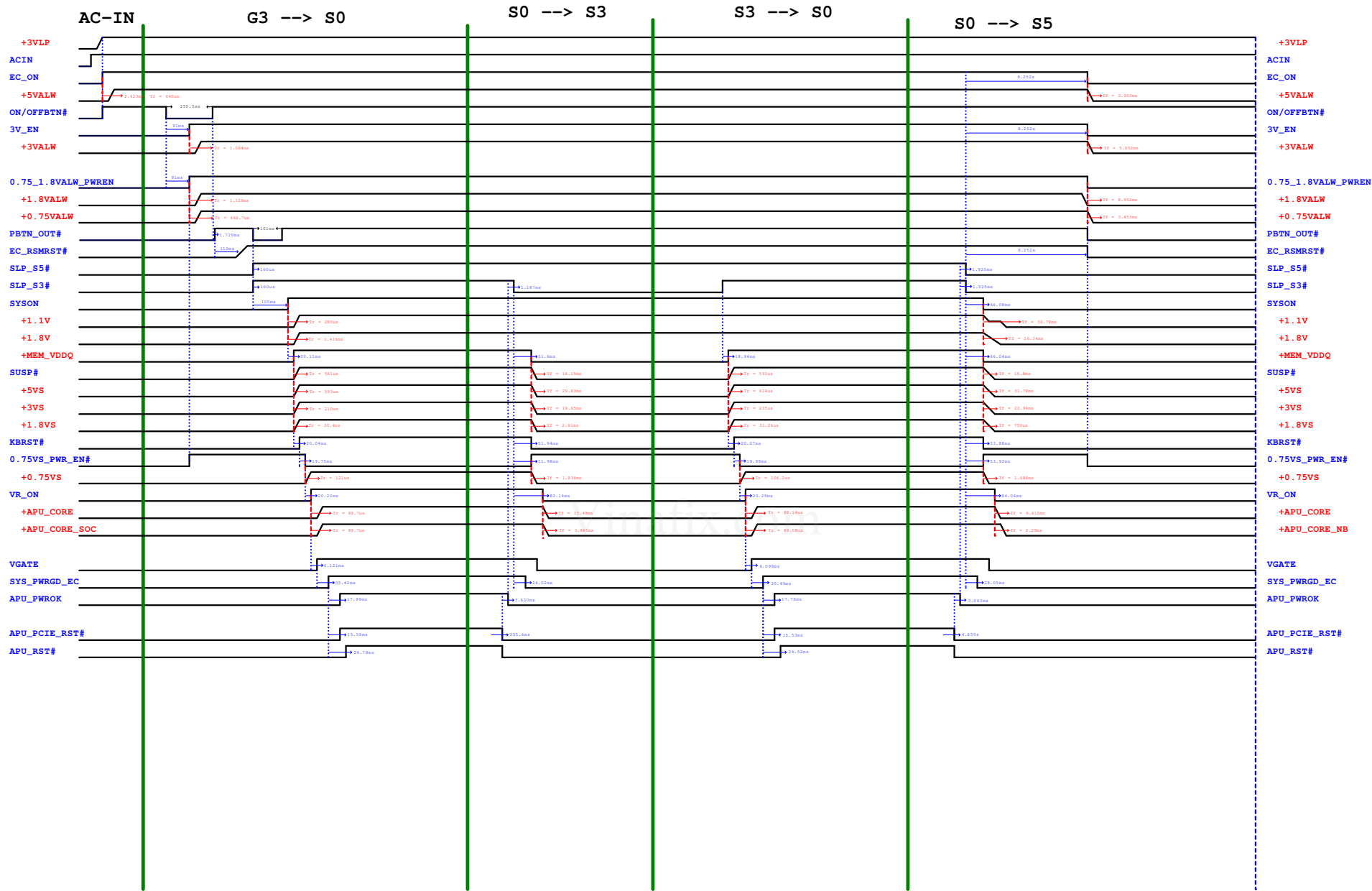
LA-K181P REV:1.0
2020-04-08

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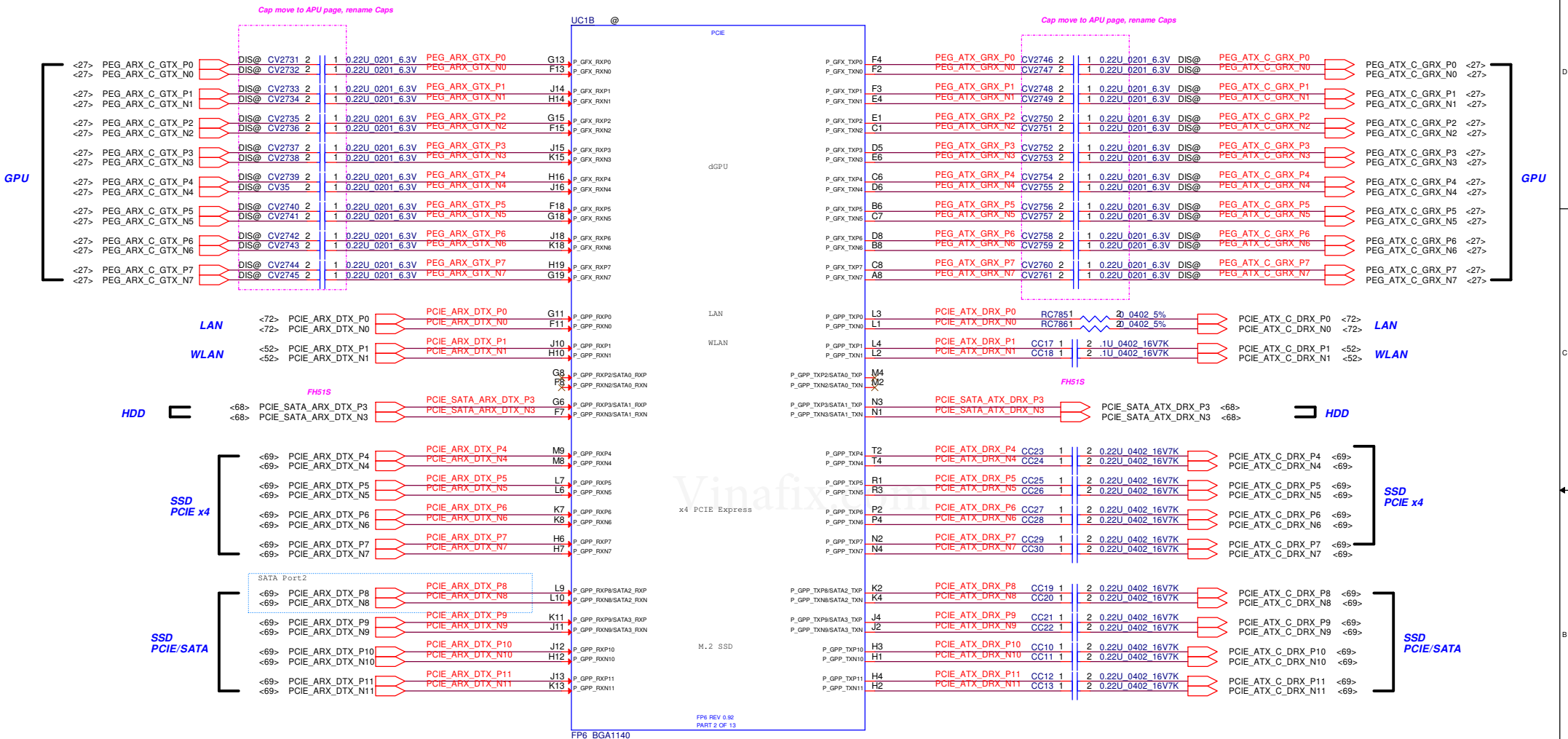
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				Rev	1.0



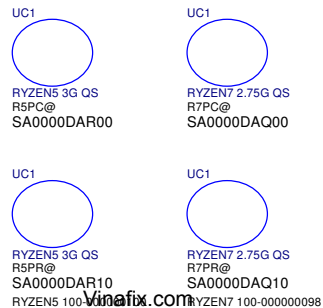




Main Func = CPU

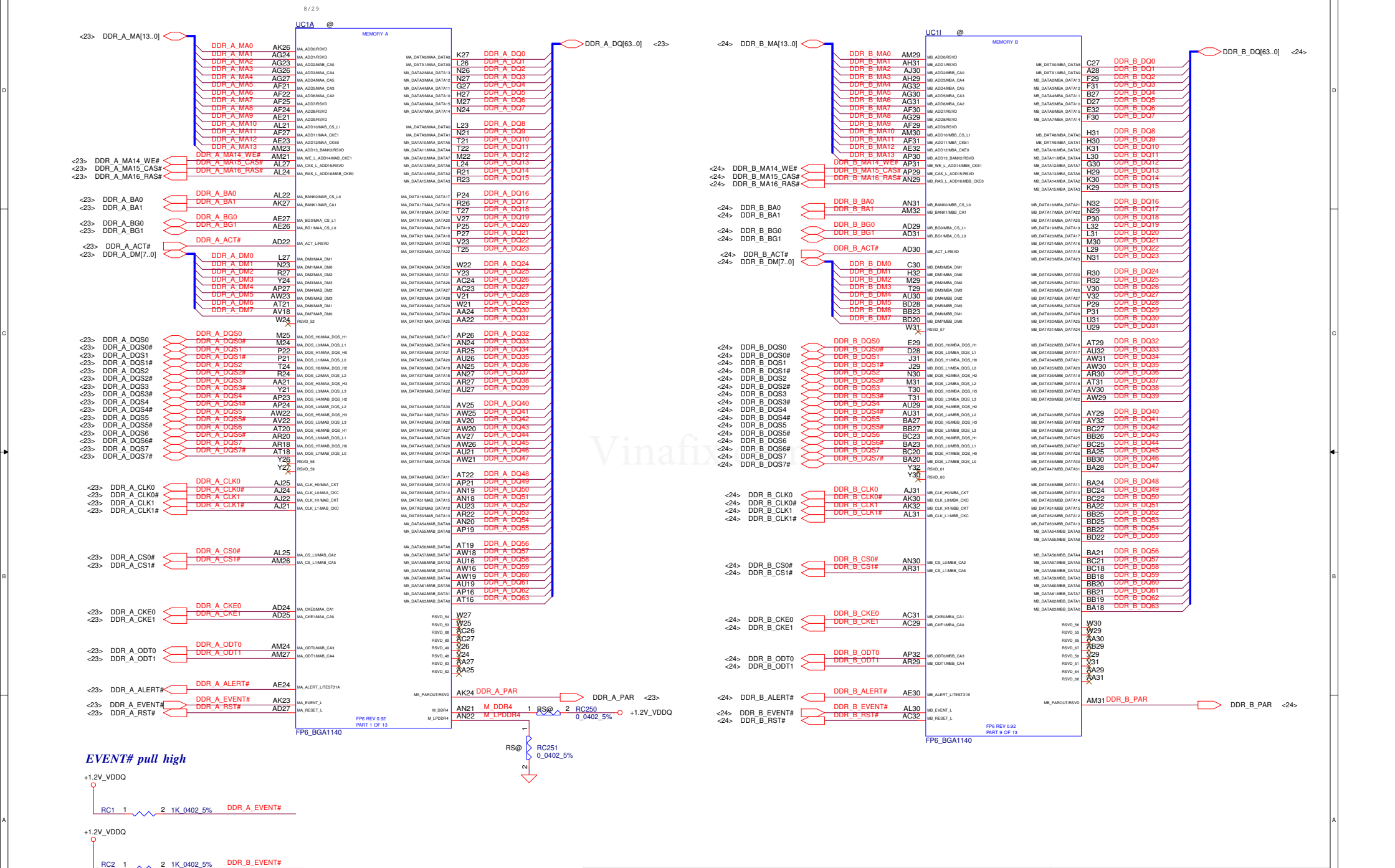


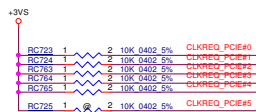
APU PN Table



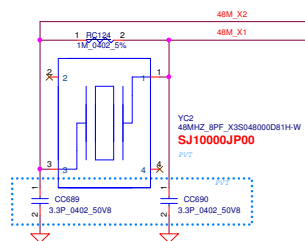
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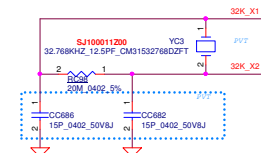




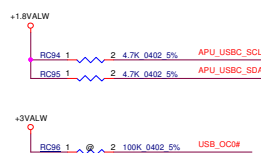
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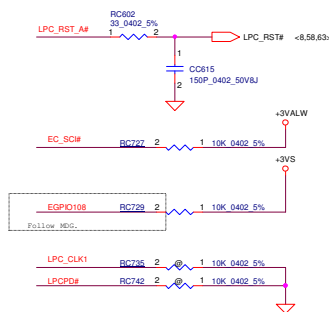
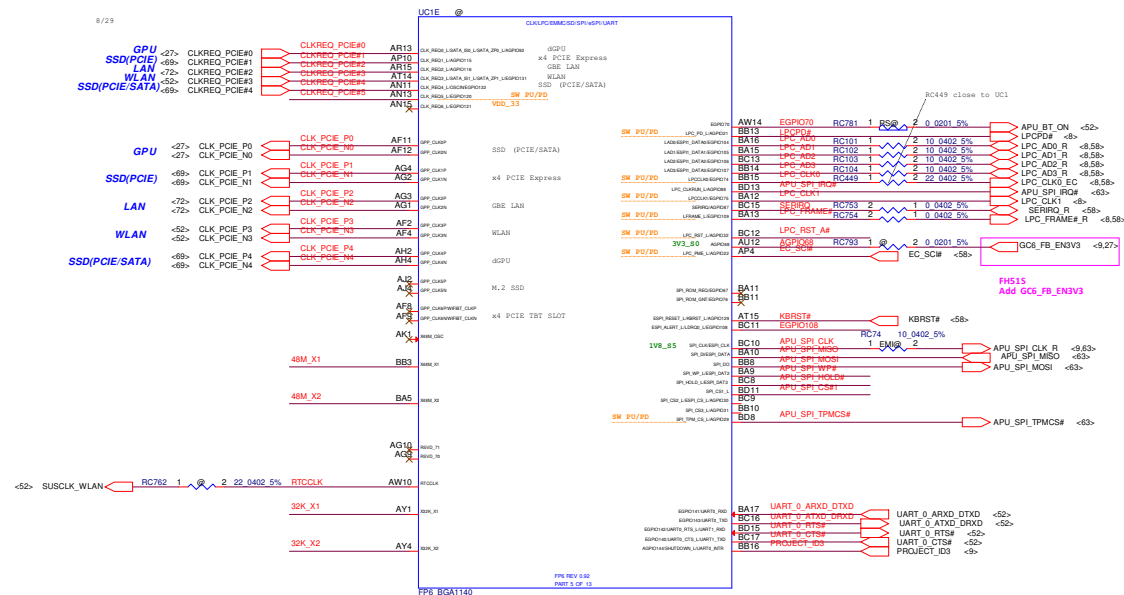
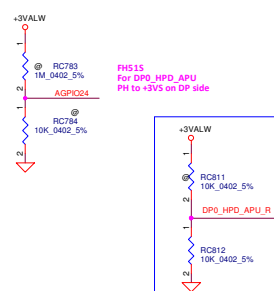
32.768KHz CRYSTAL



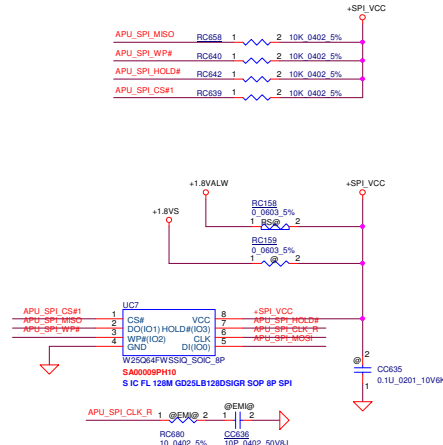
USB Function



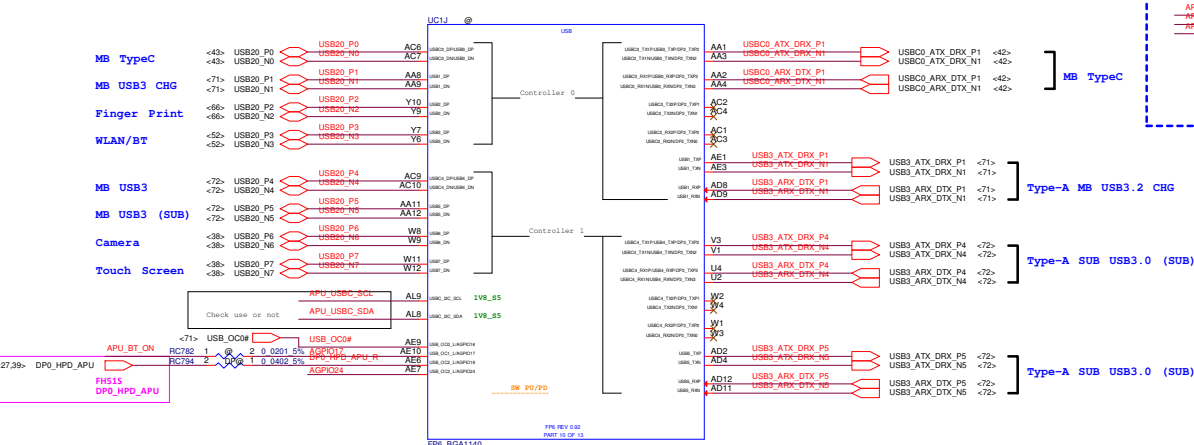
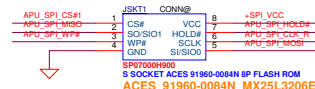
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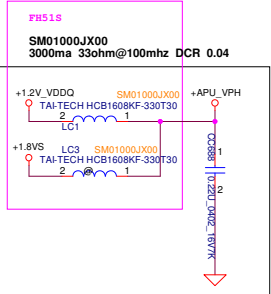
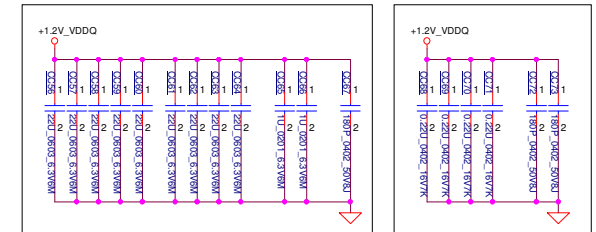
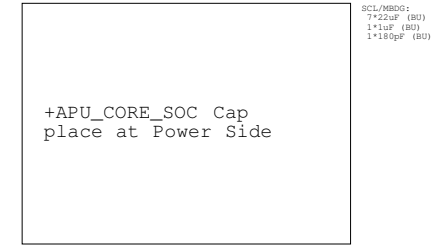
16MB SPI ROM



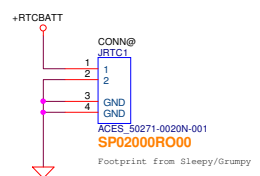
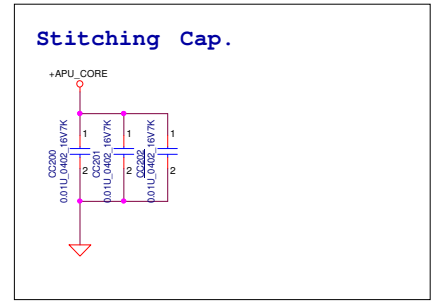
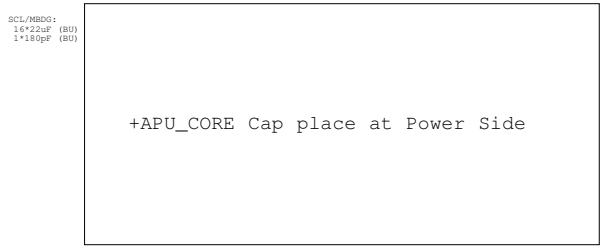
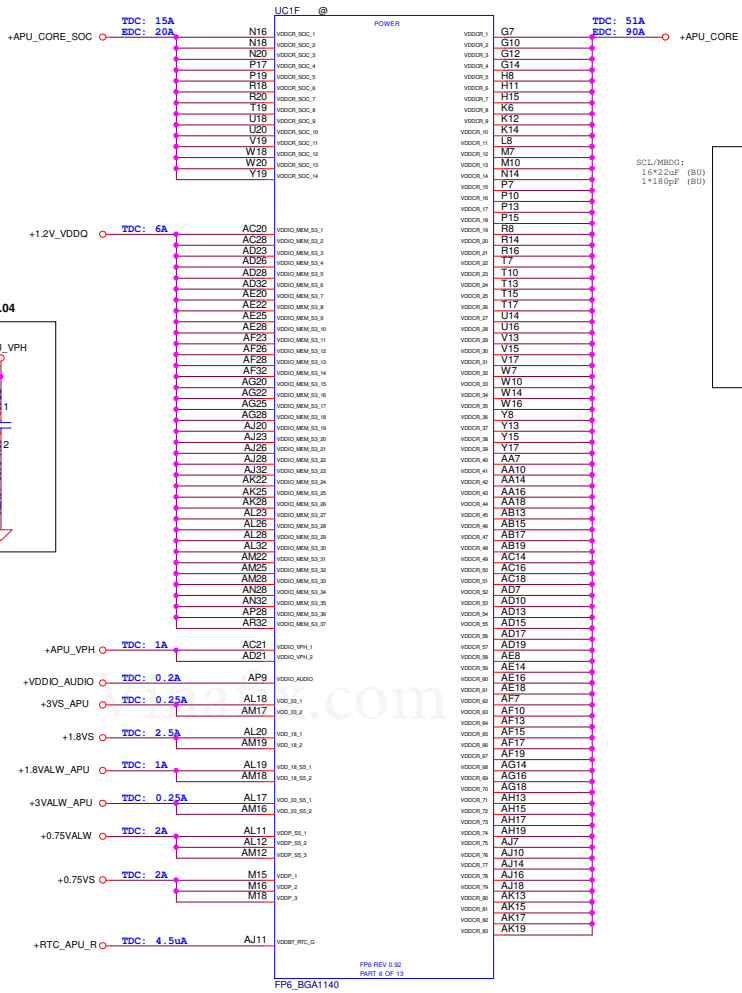
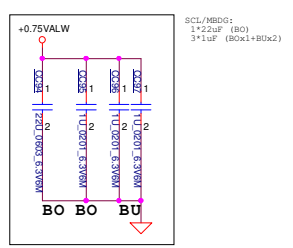
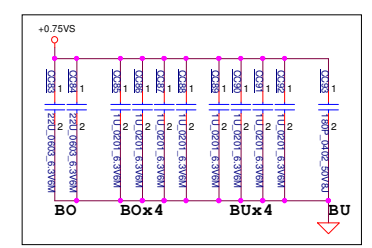
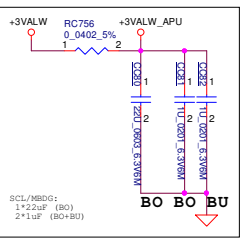
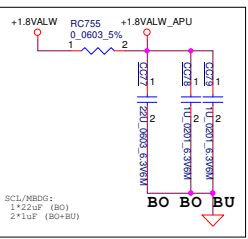
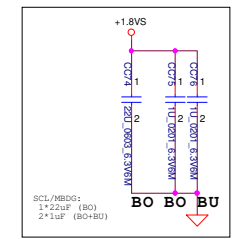
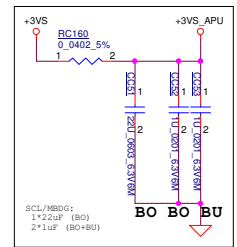
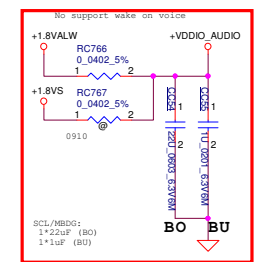
Co-lay SPI Socket with UC7



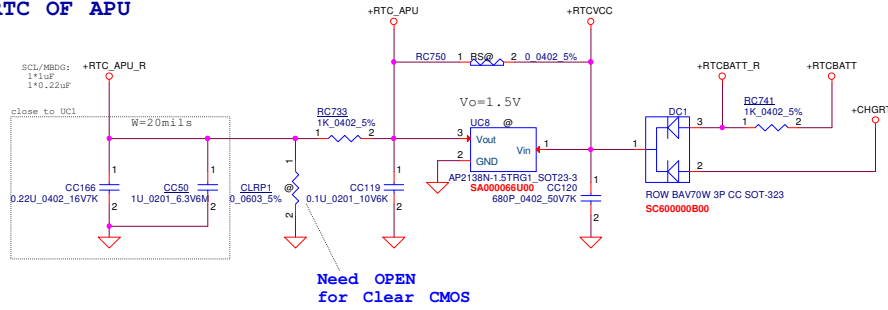
Main Func = CPU



All BU(on bottom side under SOC) ACROSS VDDIO AND VSS SPLIT



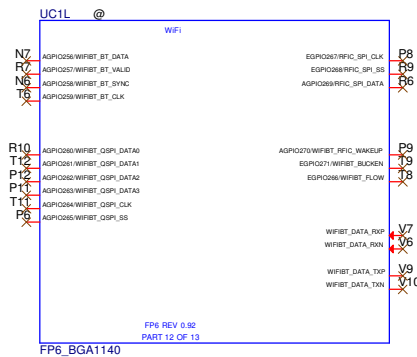
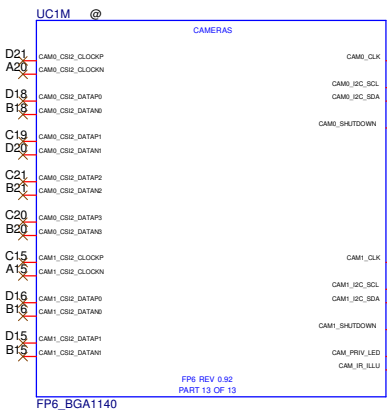
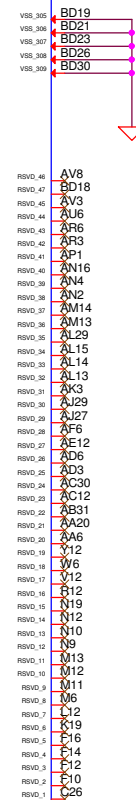
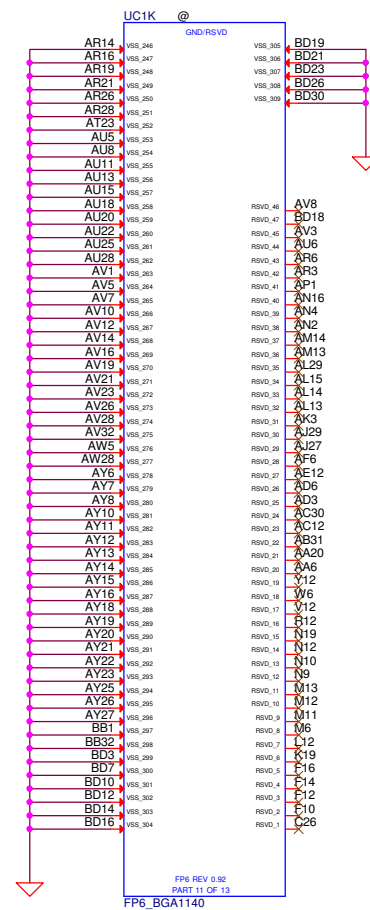
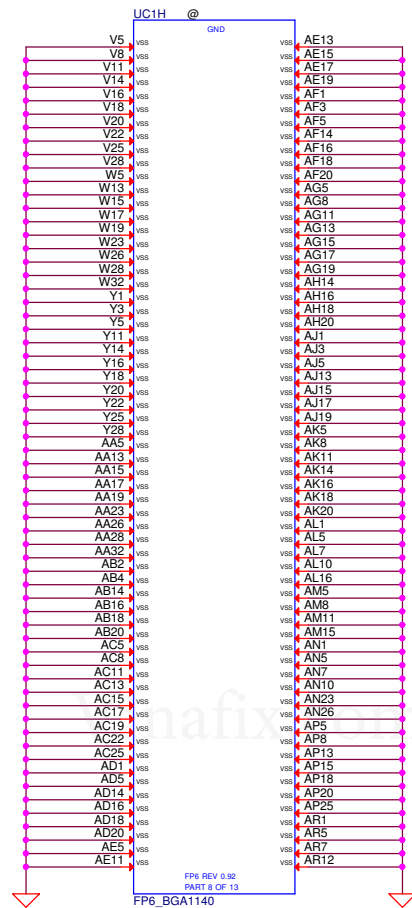
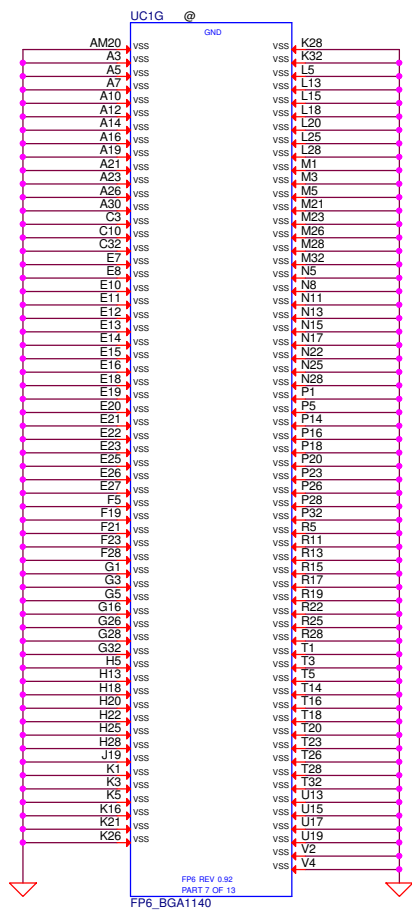
RTC OF APU



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Main Func = CPU



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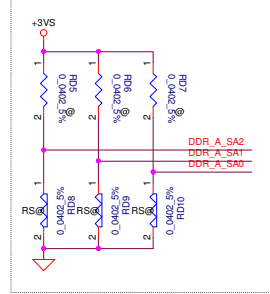
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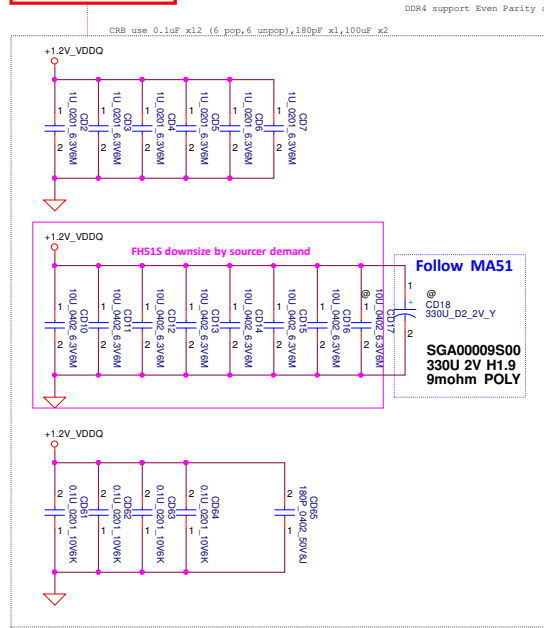
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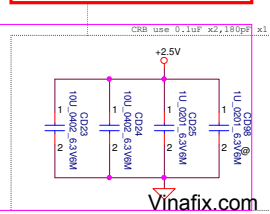
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

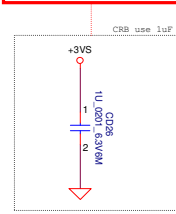


Layout Note:
Place near JDIMM1.257, 259

Layout Note:
Place near JDIMM1.255

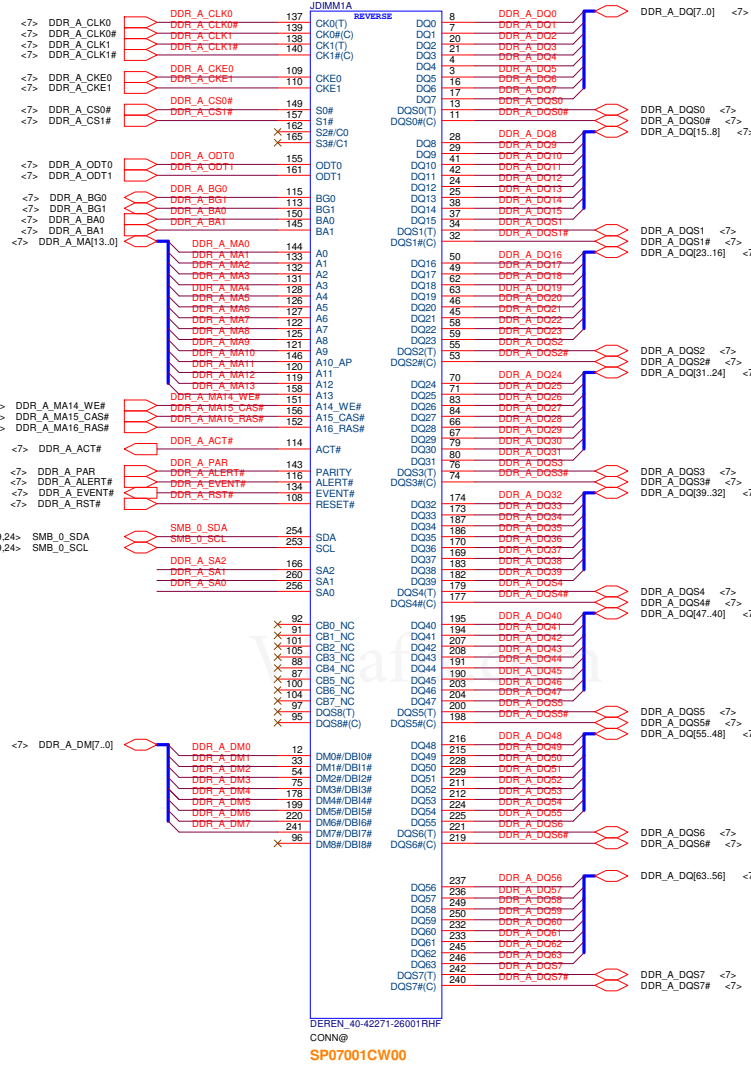


FHS15 downsized by sourcer demand



FHS15 downsized by sourcer demand

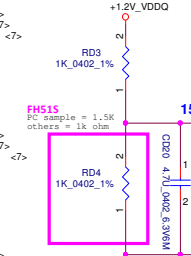
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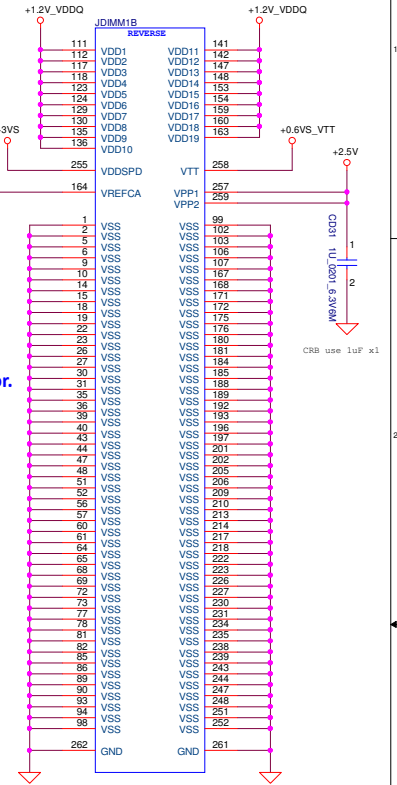
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SP07001CW00

Reverse Type
2-3A to 1 DIMMs/channel

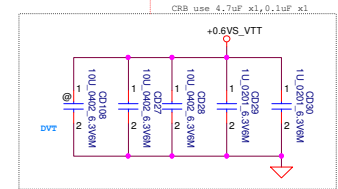
Follow CRB design



Place near to SO-DIMM connector.

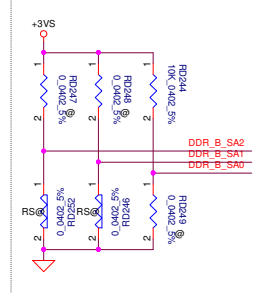


Layout Note:
Place near JDIMM1.258



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Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

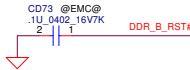
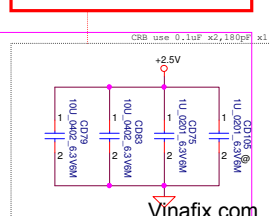
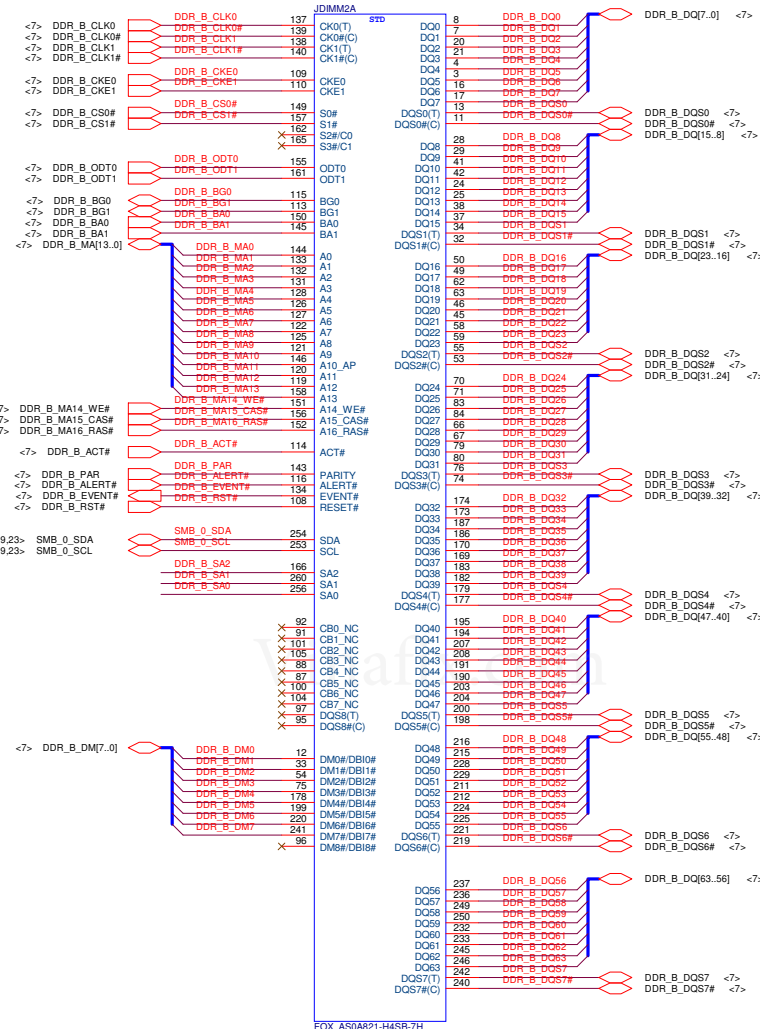
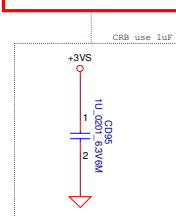


Figure 10 illustrates the power plane layout for the HPS15, showing three cross-sectional views of the layout. The top view shows the layout for +1.2V_VDDQ, with components like CD104, CD103, CD102, CD101, CD100, CD99, CD98, CD97, CD96, CD95, CD94, CD93, CD92, CD91, and CD90. The middle view shows the layout for +1.2V_VDDQ, with components like CD104, CD103, CD102, CD101, CD100, CD99, CD98, CD97, CD96, CD95, CD94, CD93, CD92, CD91, and CD90. The bottom view shows the layout for +1.2V_VDDQ, with components like CD104, CD103, CD102, CD101, CD100, CD99, CD98, CD97, CD96, CD95, CD94, CD93, CD92, CD91, and CD90.

Layout Note:
Place near JDIMM2.255



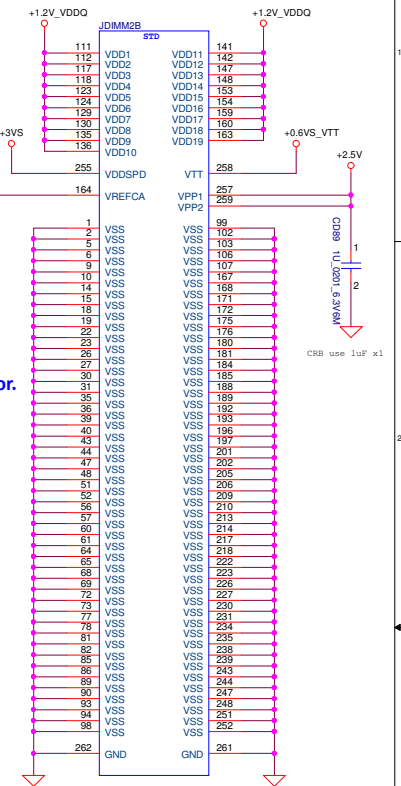
FH51S downsize by sourcer demand



FOX_AS0A821-H4SB-7H
CONN@
SP07001HW00

Symbol follow EH5AW (Lada

Place near to SO-DIMM connector.

[illegible]

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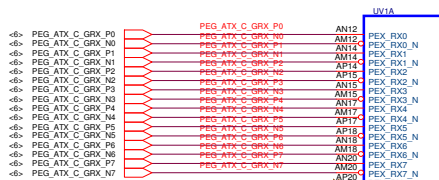
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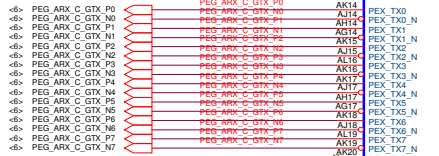
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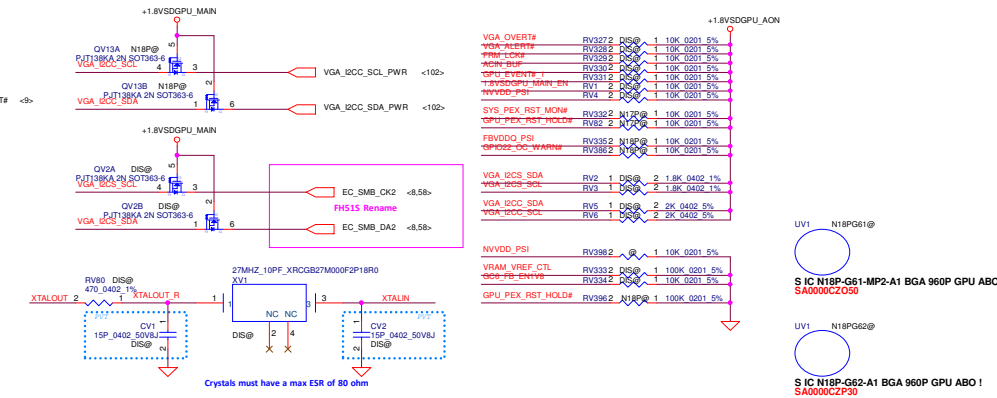
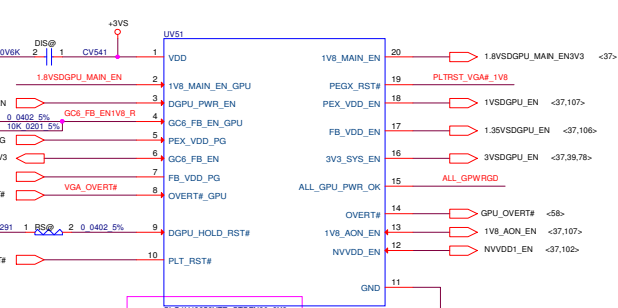
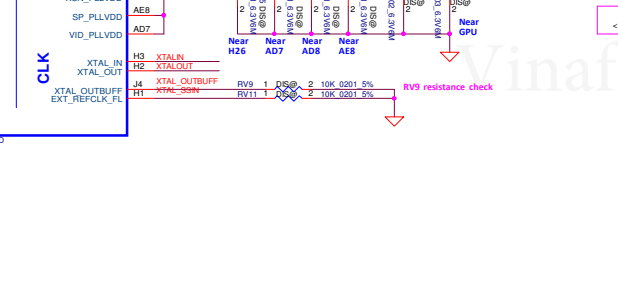
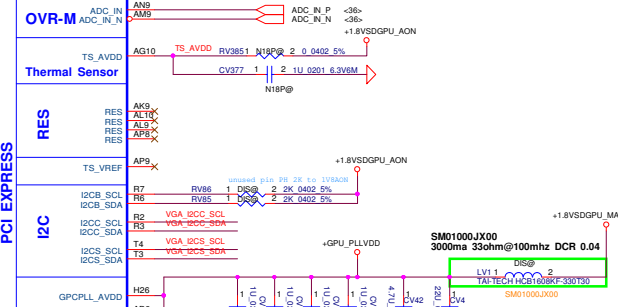
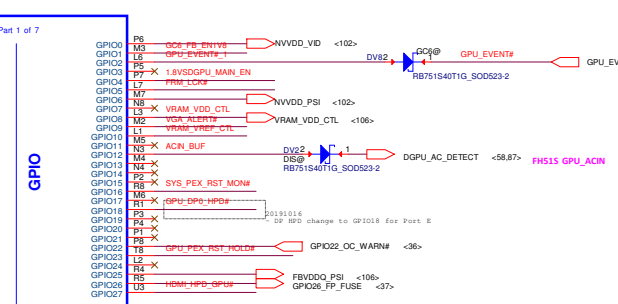
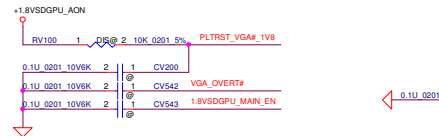
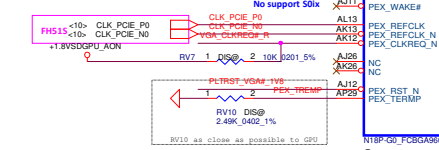
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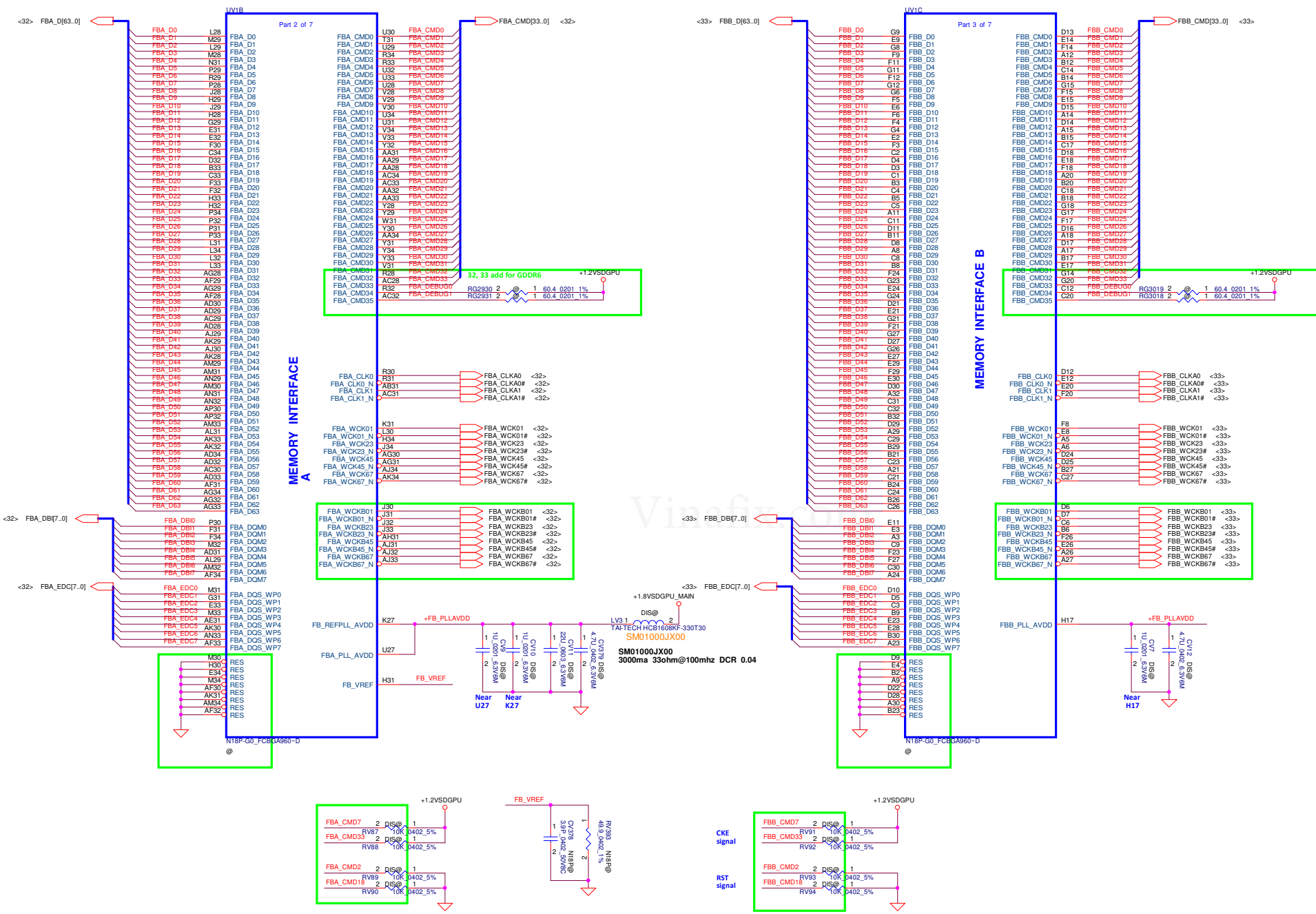


FH515 Support PEG x8 only

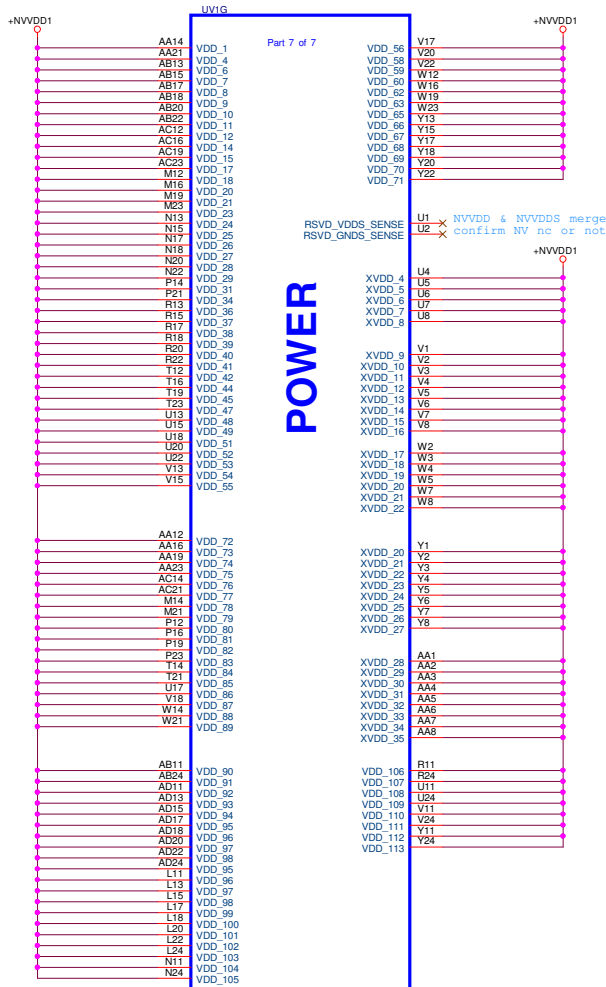


FH515 Support PEG x8 only





N17P VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2

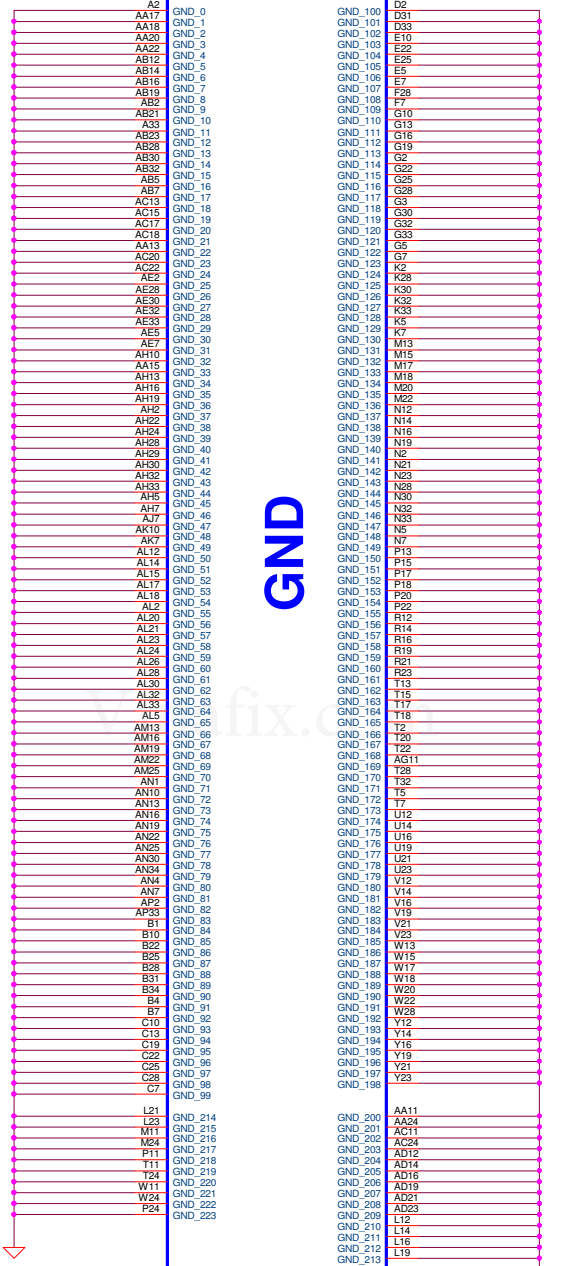


POWER

N18P-G0_FCBGA960-D
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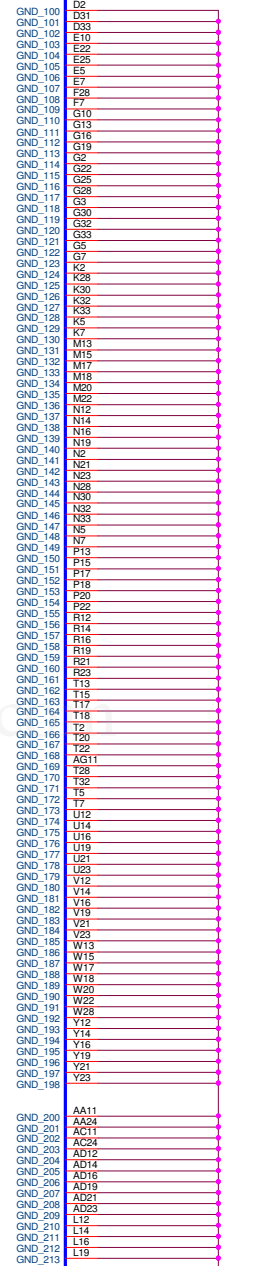
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Part 6 of 7

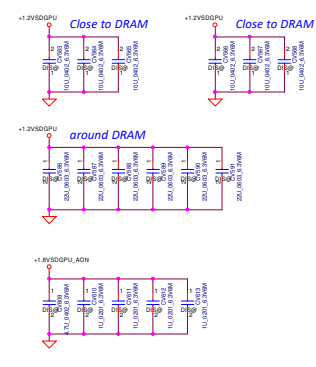
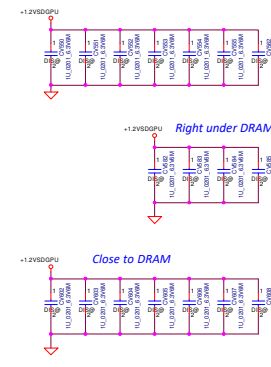
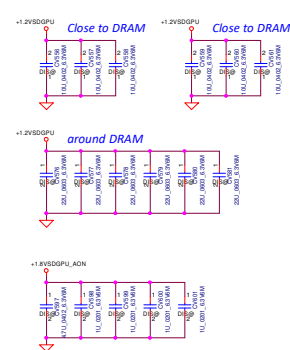
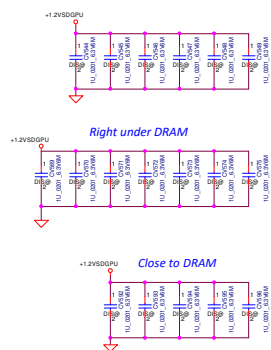
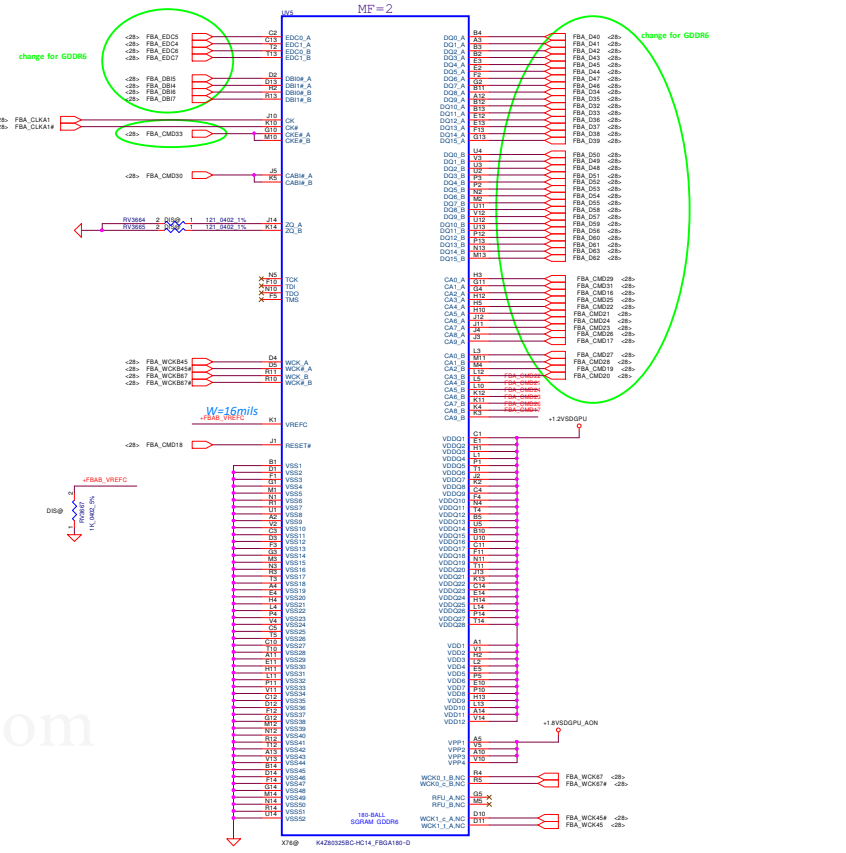
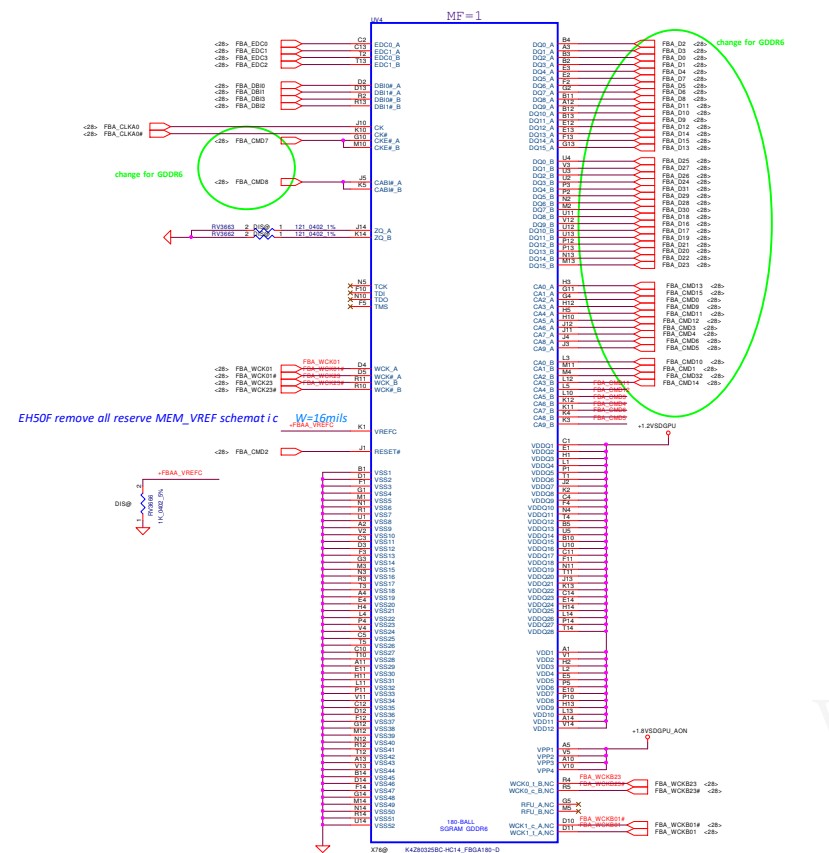


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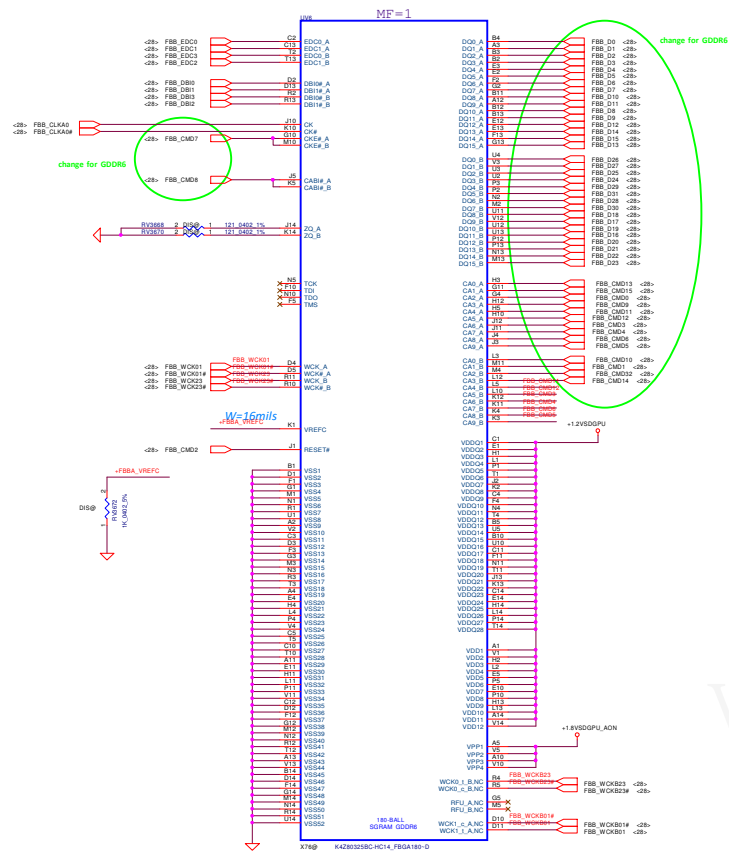
N18P-G0_FCBGA960-D
@



NC
AH11 RV3952 N17P@ 1.0 0.0402.5%
C16
W32
GND_OPT
GND_OPT



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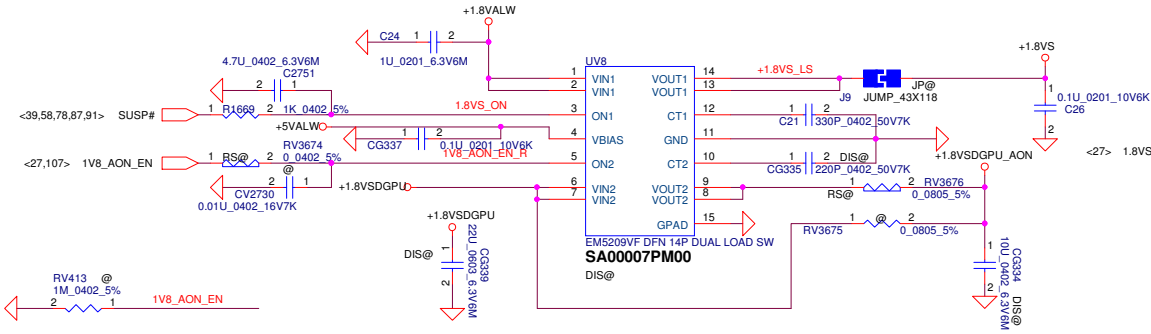
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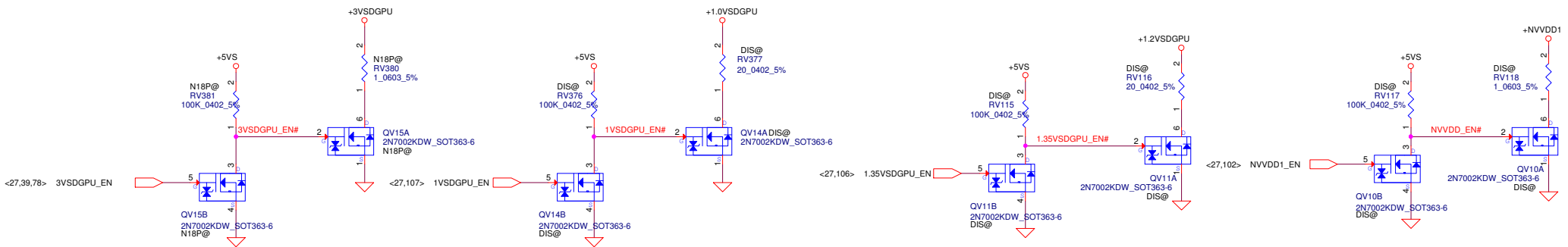
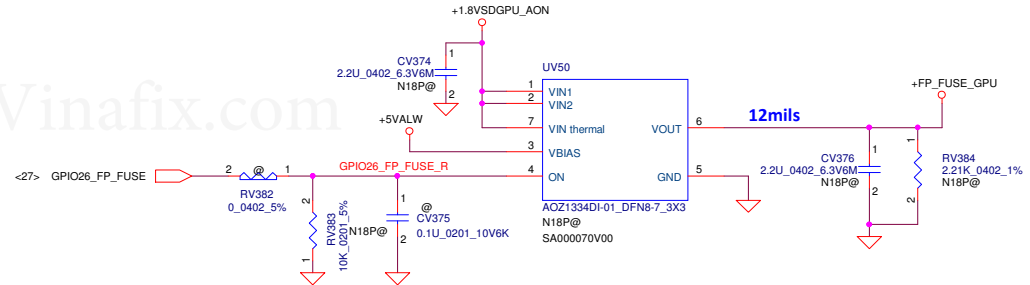
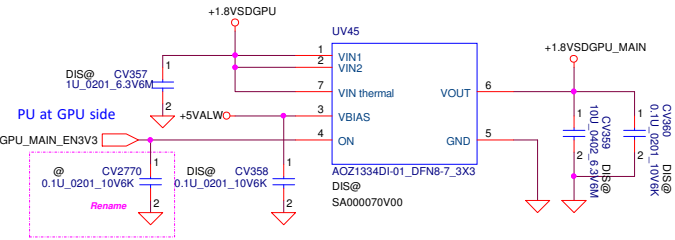
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+1.8V_AON/+1.8VS

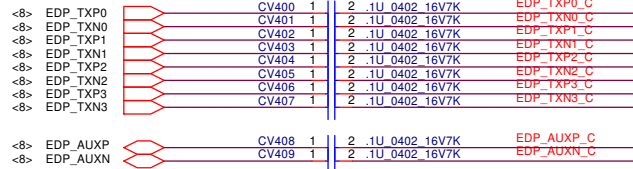
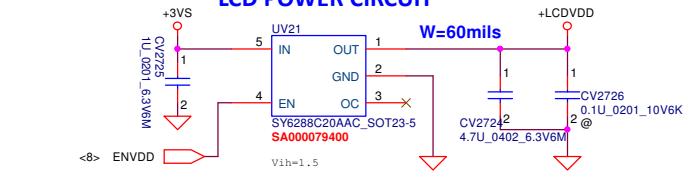


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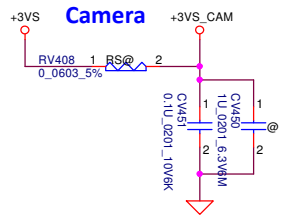


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LCD POWER CIRCUIT

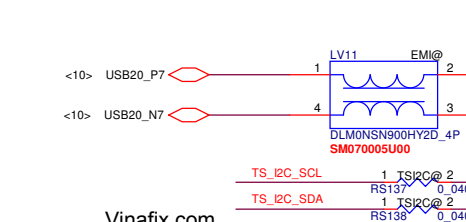
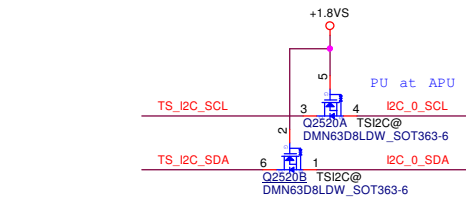
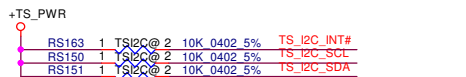
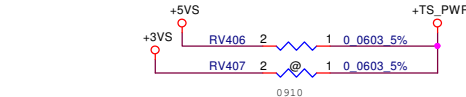


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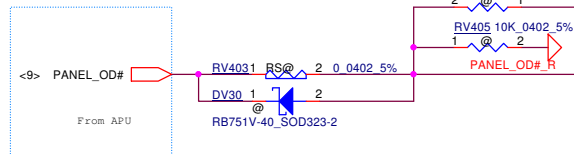
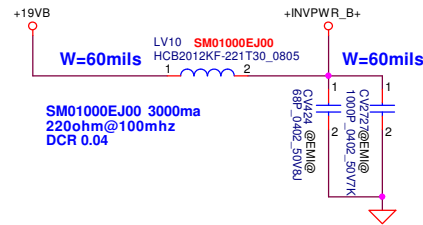


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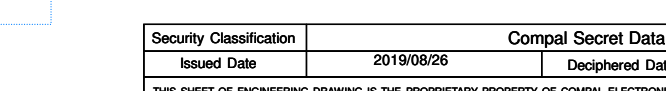
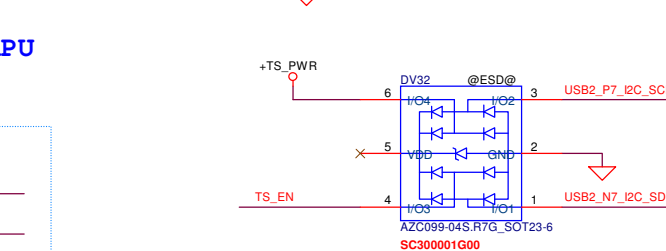
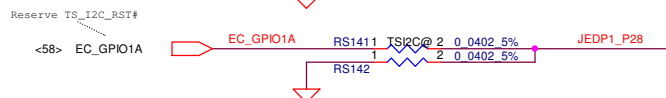
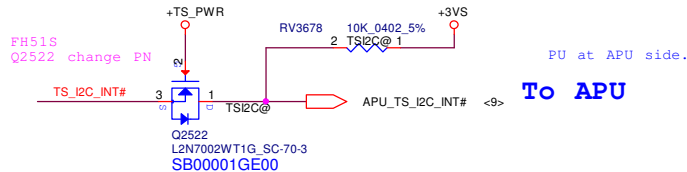
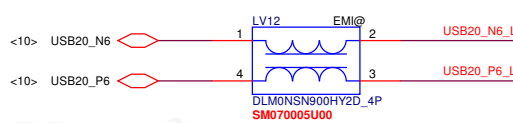
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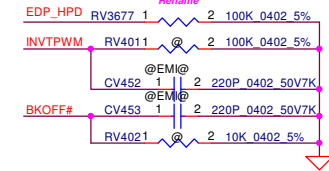
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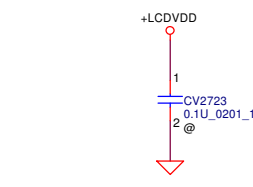
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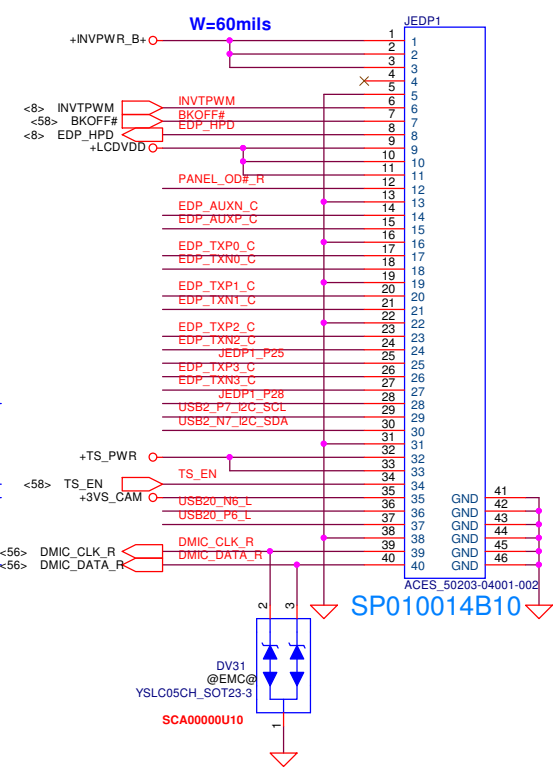
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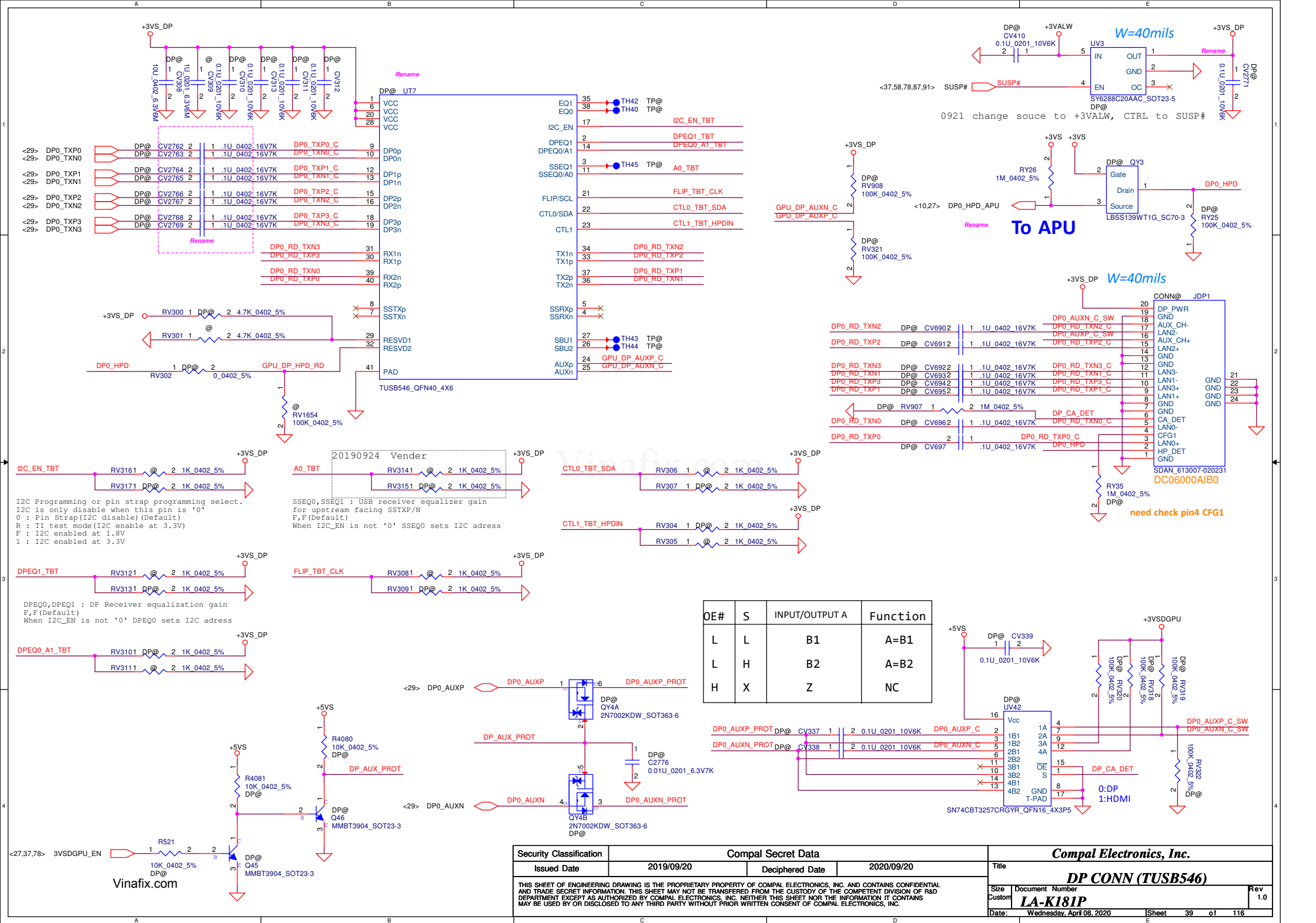


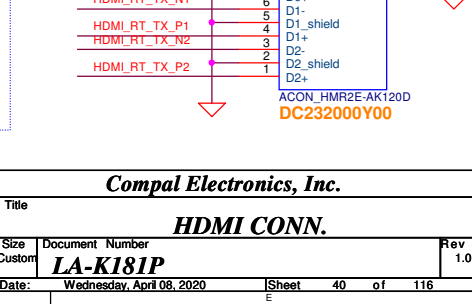
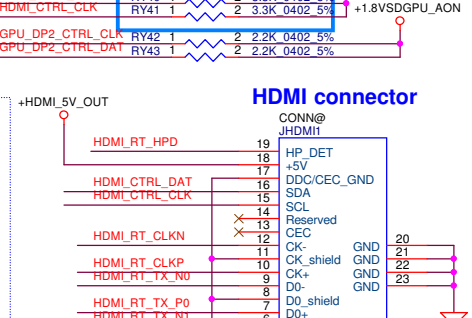
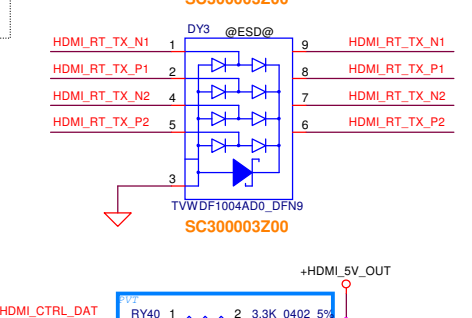
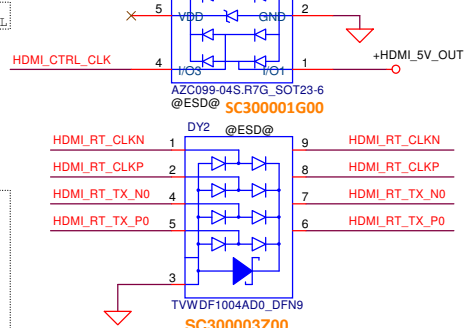
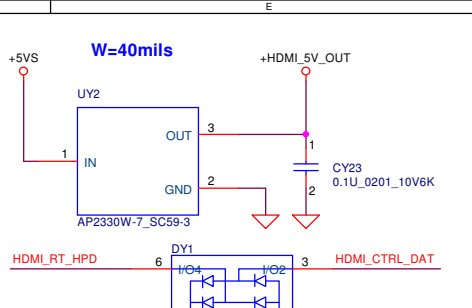
LED PANEL Conn.



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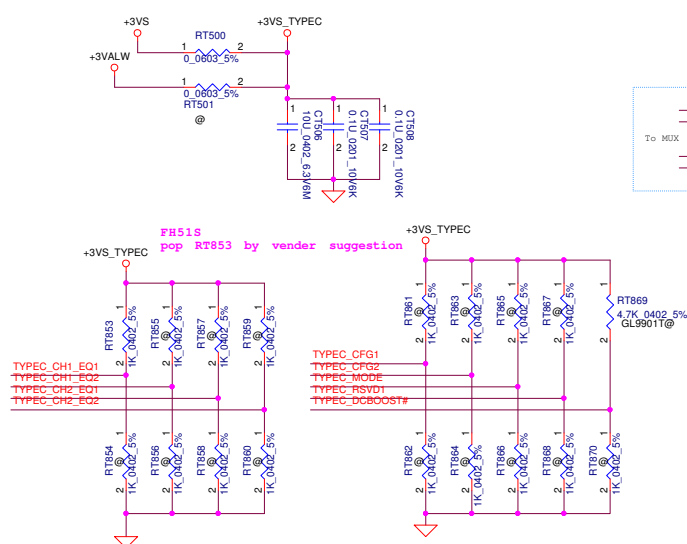
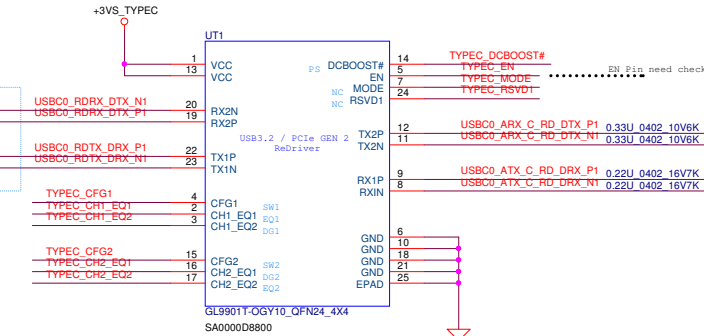
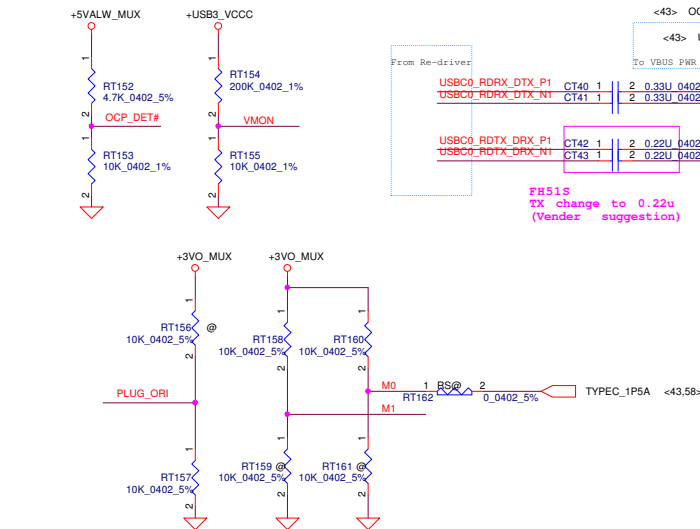
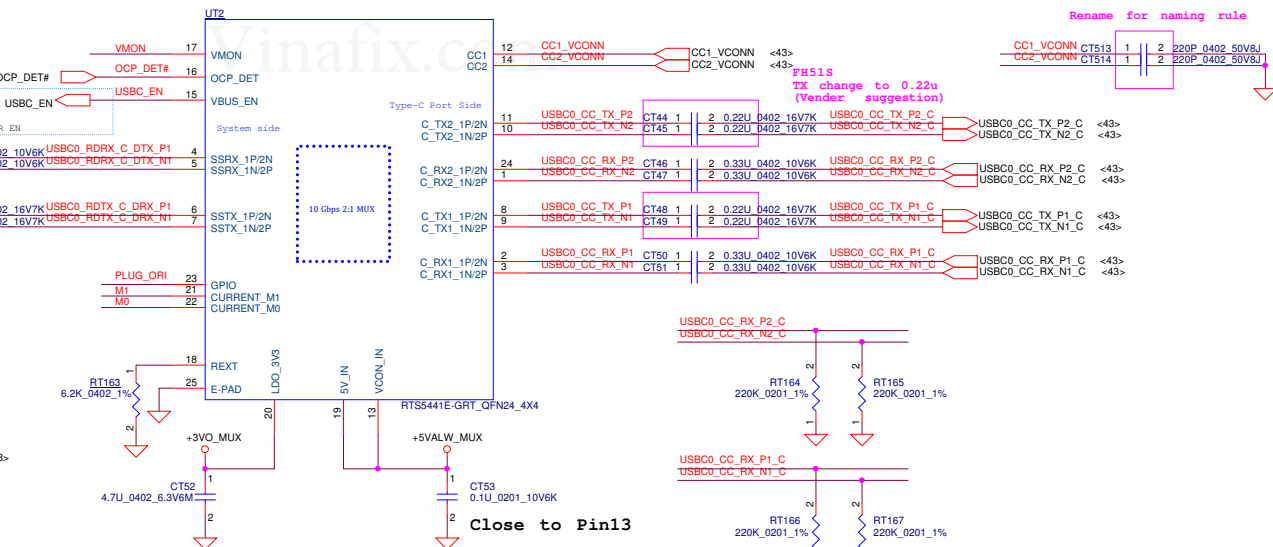
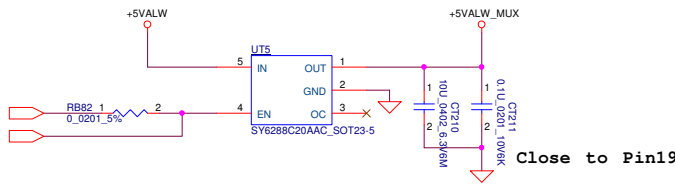


Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .



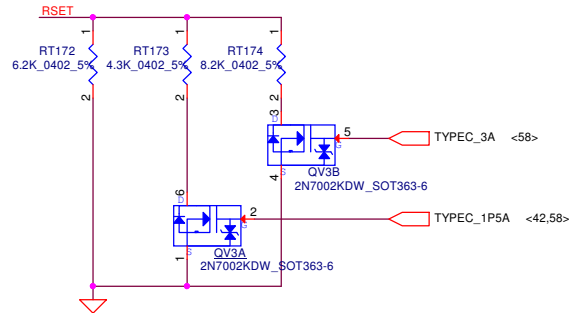
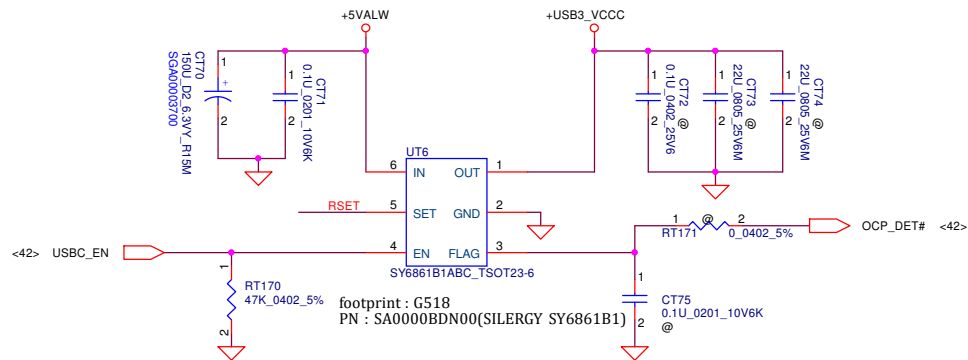
2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H



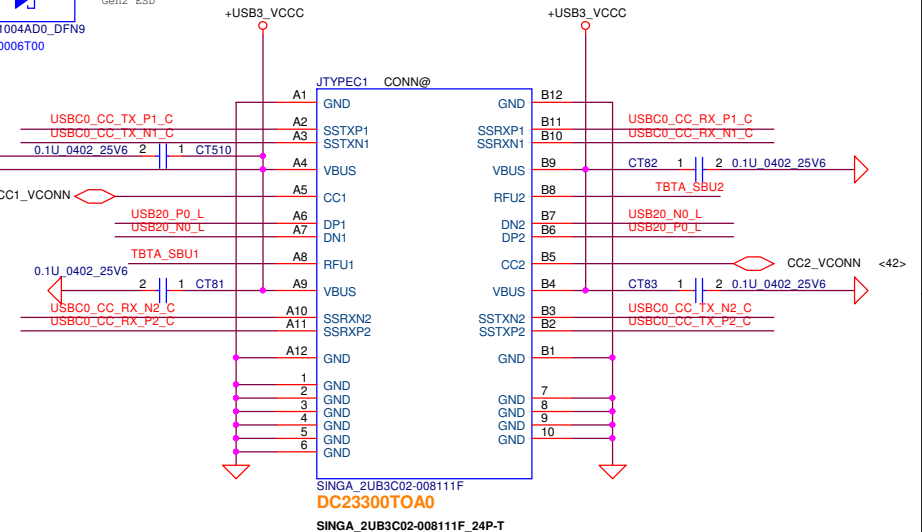
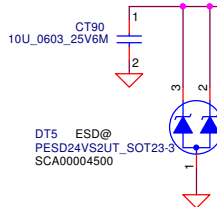
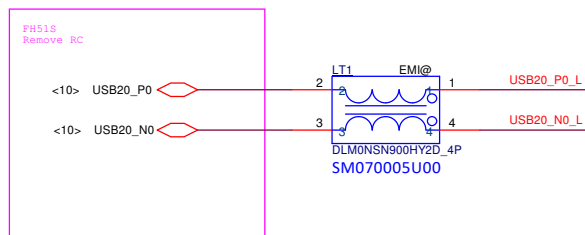
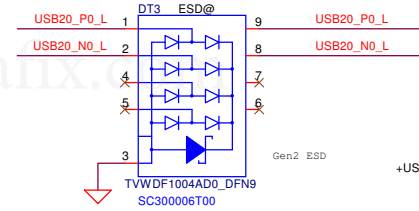
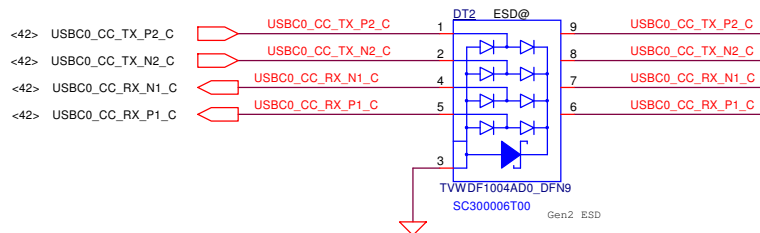
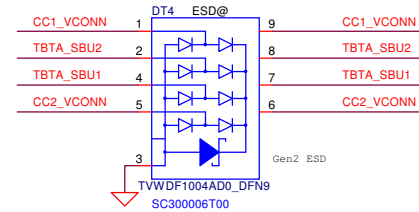
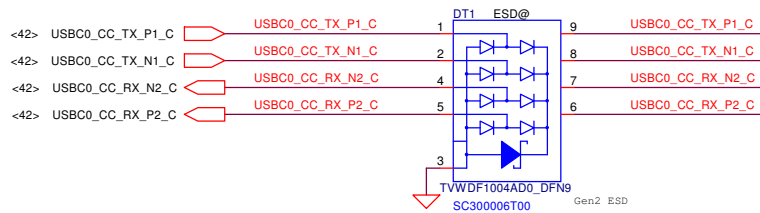
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

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SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20mil trace width.

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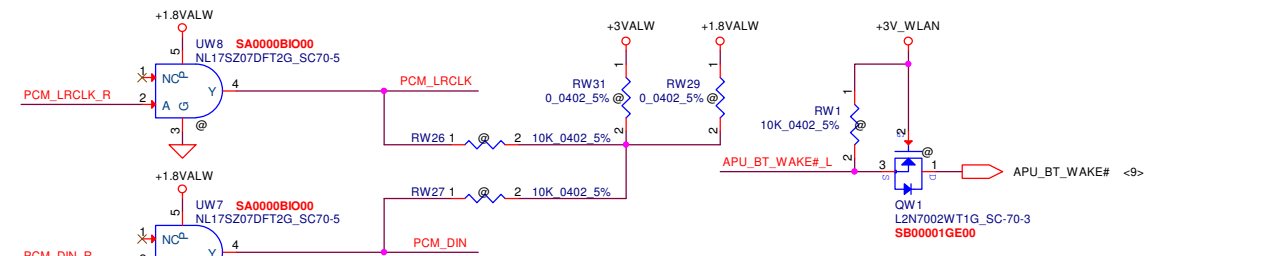
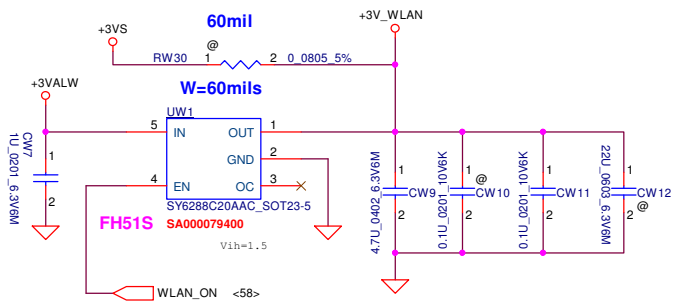
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Wireless LAN

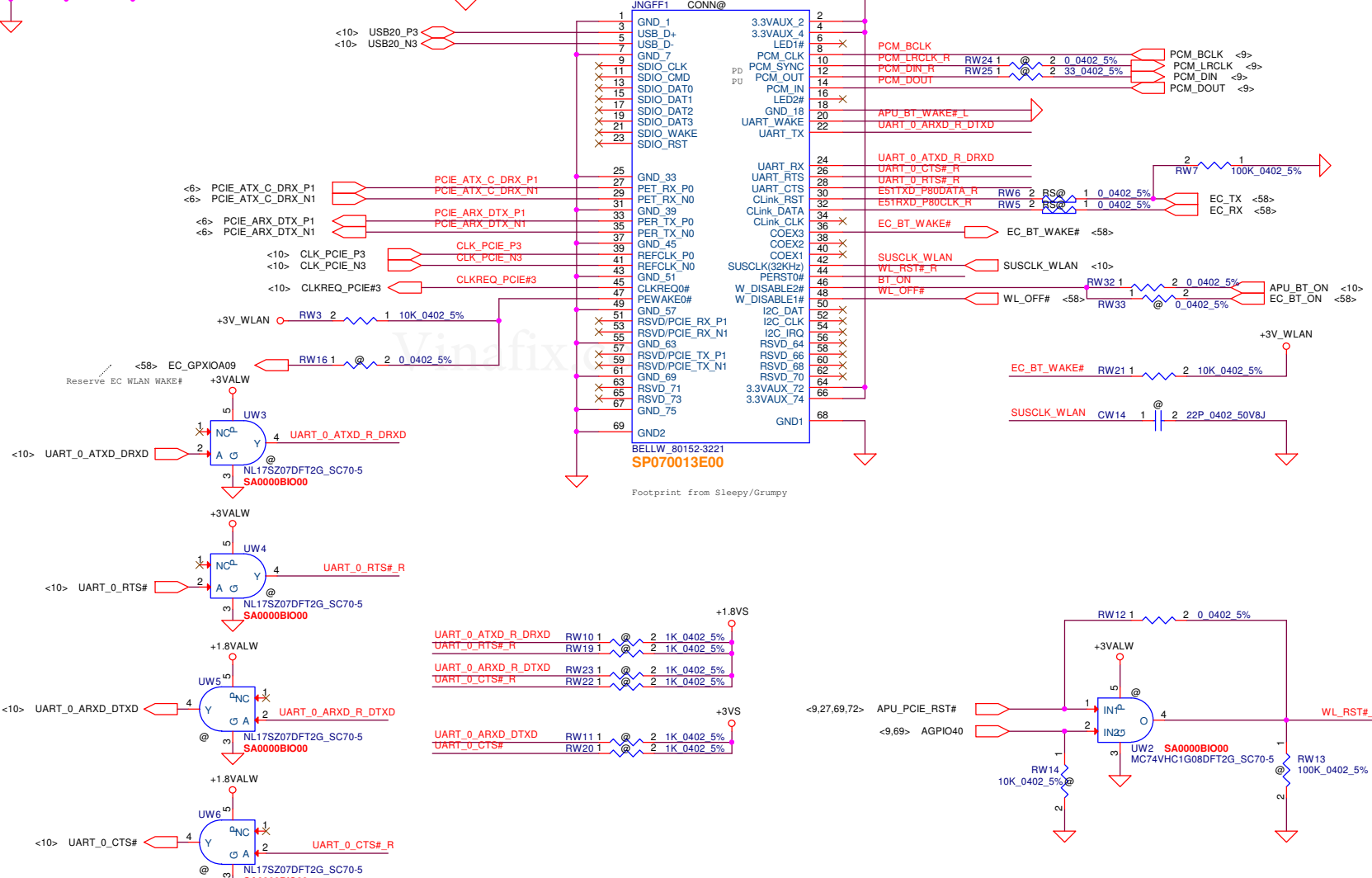
0912



KEY E

NGFF WL+BT (KEY E)

74	1.3V	GND	75
72	1.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PEWake#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ#	GND	69
66	UM_SWP/PERST#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O/3.3)	GND	63
60	IDC CLK (I/O/3.3)	Reserved/PETn1	61
58	IDC DATA (I/O/3.3)	Reserved/PETp1	59
56	WL_DISABLE#1 (O/I/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O/I/3.3V)	PEWake# (O/I/3.3V)	55
52	PERST# (O/I/3.3V)	CLKREQ# (O/I/3.3V)	53
50	SUSCLK(32KHz) (O/I/3.3V)	GND	51
48	COEX1 (I/O/1.8V)	REFCLKN0	49
46	COEX2 (O/I/1.8V)	REFCLKP0	47
44	COEX3 (I/O/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O/I/1.8V)	PETn0	37
34	UART CTS (I/O/1.8V)	PETp0	35
32	UART Tx (O/I/1.8V)	GND	33
22	UART Rx (I/O/1.8V)	SDIO Reserve (I/O/1.8V)	23
20	UART Wake# (I/O/3.3V)	SDIO Wake# (I/O/1.8V)	21
18	GND	SDIO DAT#0 (O/I/1.8V)	19
16	LED#2 (I/IO)	SDIO DAT#1 (O/I/1.8V)	17
14	PCM_OUT/ISD_OUT (O/I/1.8V)	SDIO DAT#2 (O/I/1.8V)	15
12	PCM_IN/ISD_IN (I/O/1.8V)	SDIO CMD#0 (O/I/1.8V)	13
10	PCM_SYNC/ISD_VS (O/I/1.8V)	SDIO CMD#1 (O/I/1.8V)	11
8	PCM_CLK/ISD_SCK (O/I/1.8V)	SDIO CLK (O/I/1.8V)	9
6	LED#1 (I/IO)	GND	7
4	1.3V	USB_D-	5
2	1.3V	USB_D+	3
		GND	1



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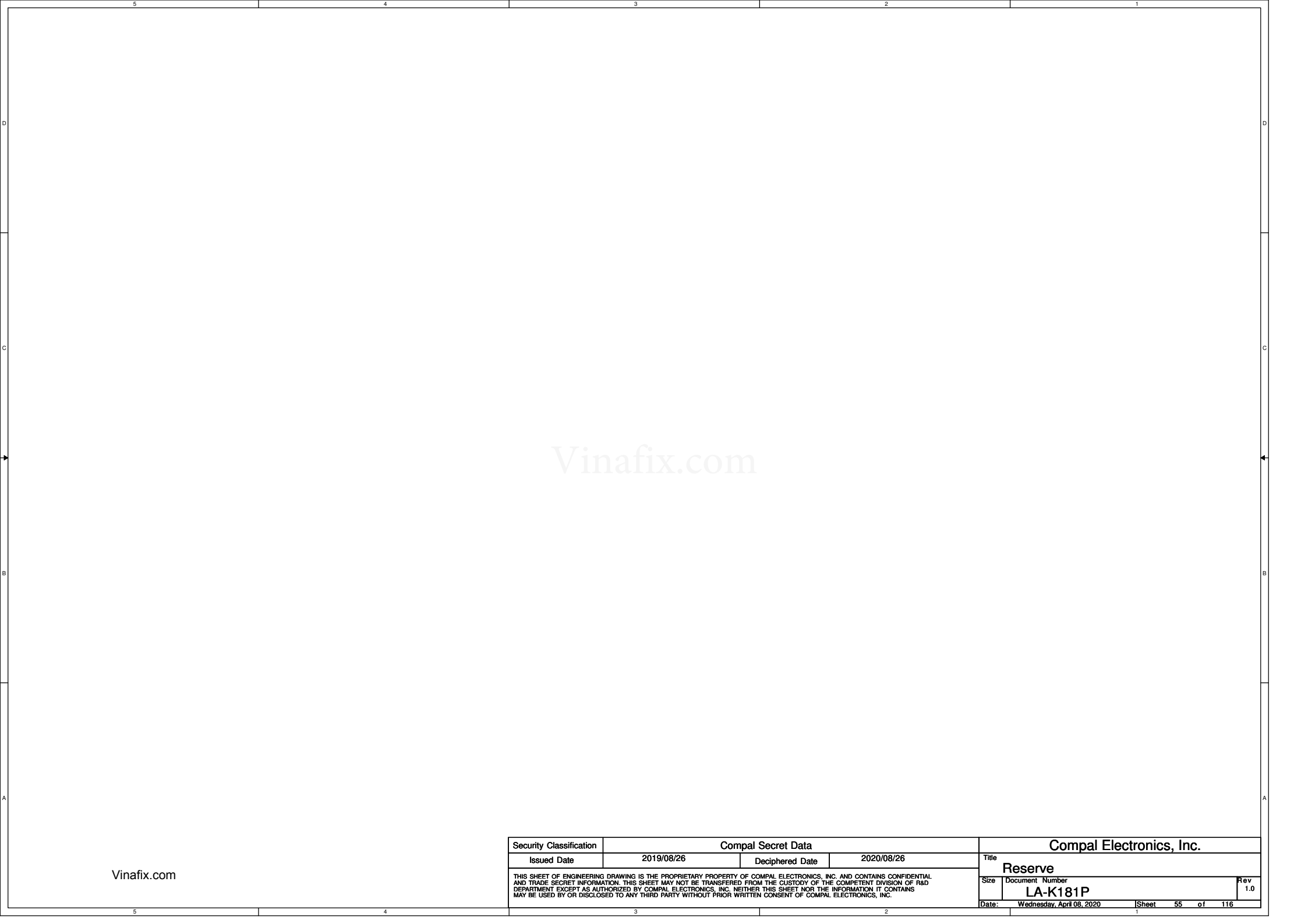
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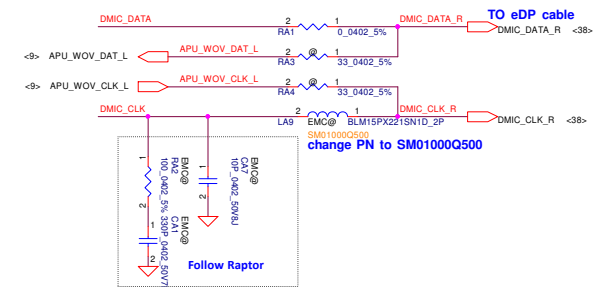
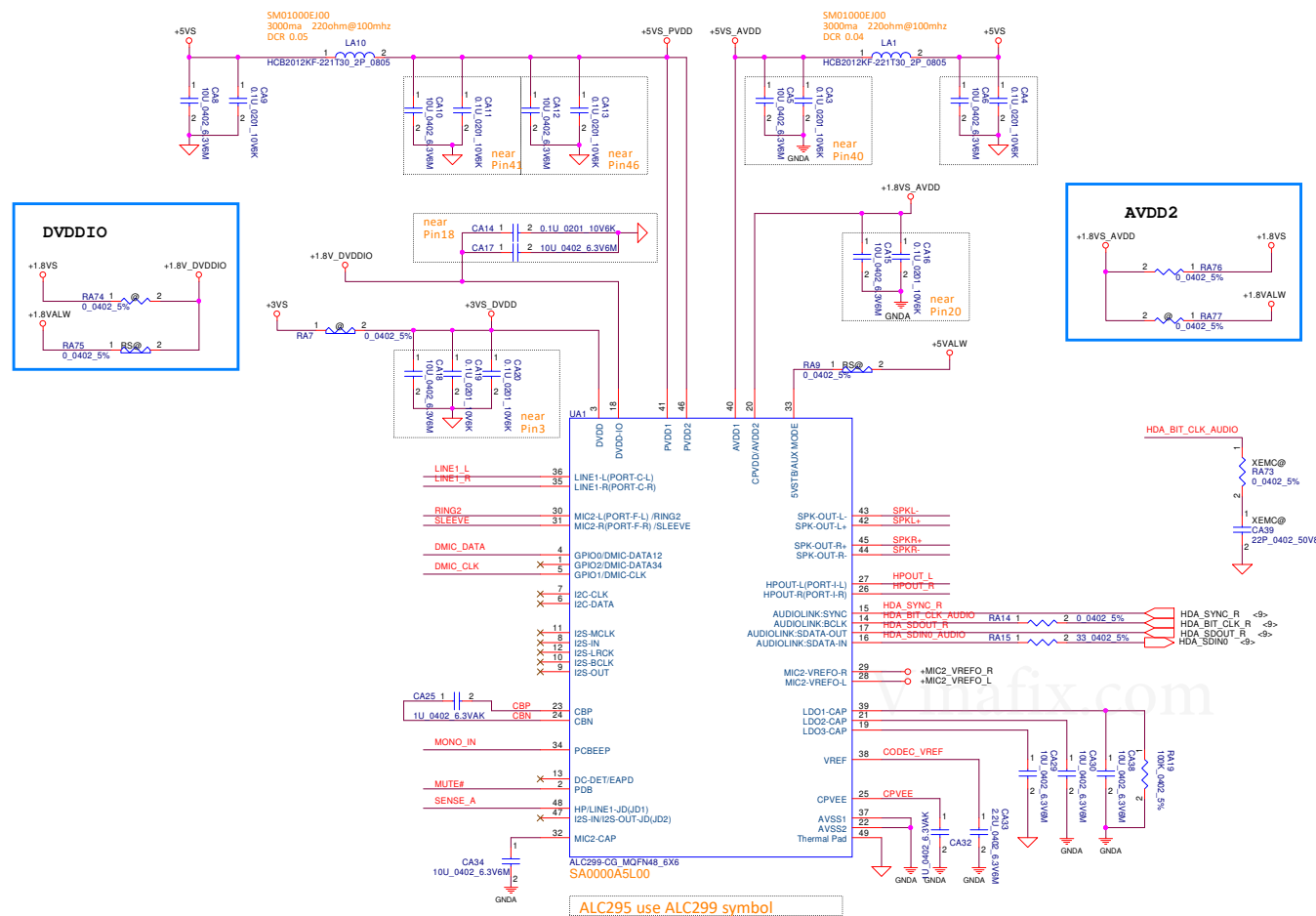
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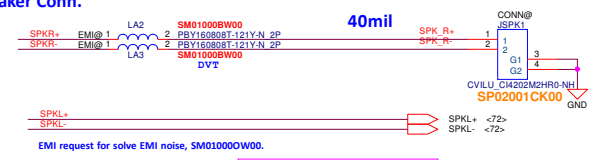
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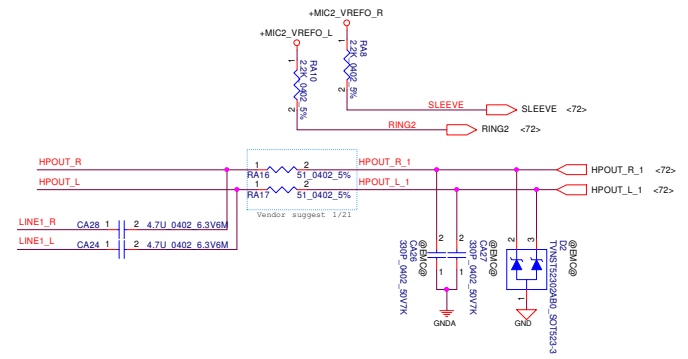
HD Audio Codec



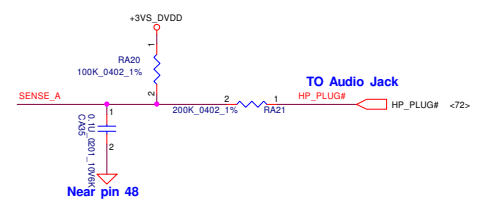
Int. Speaker Conn.



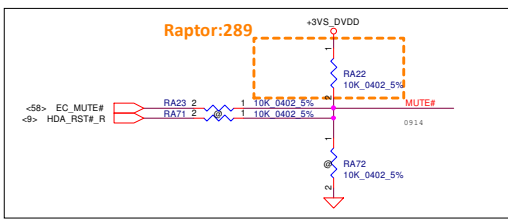
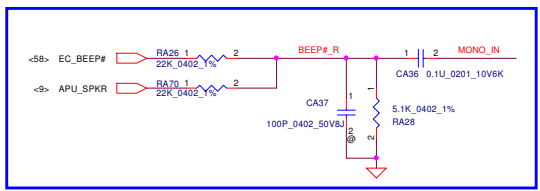
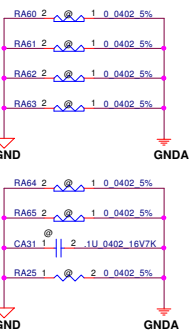
Headphone Out



JACK Detect



JD1	
HP-JD	LINE1-JD
200K	100K

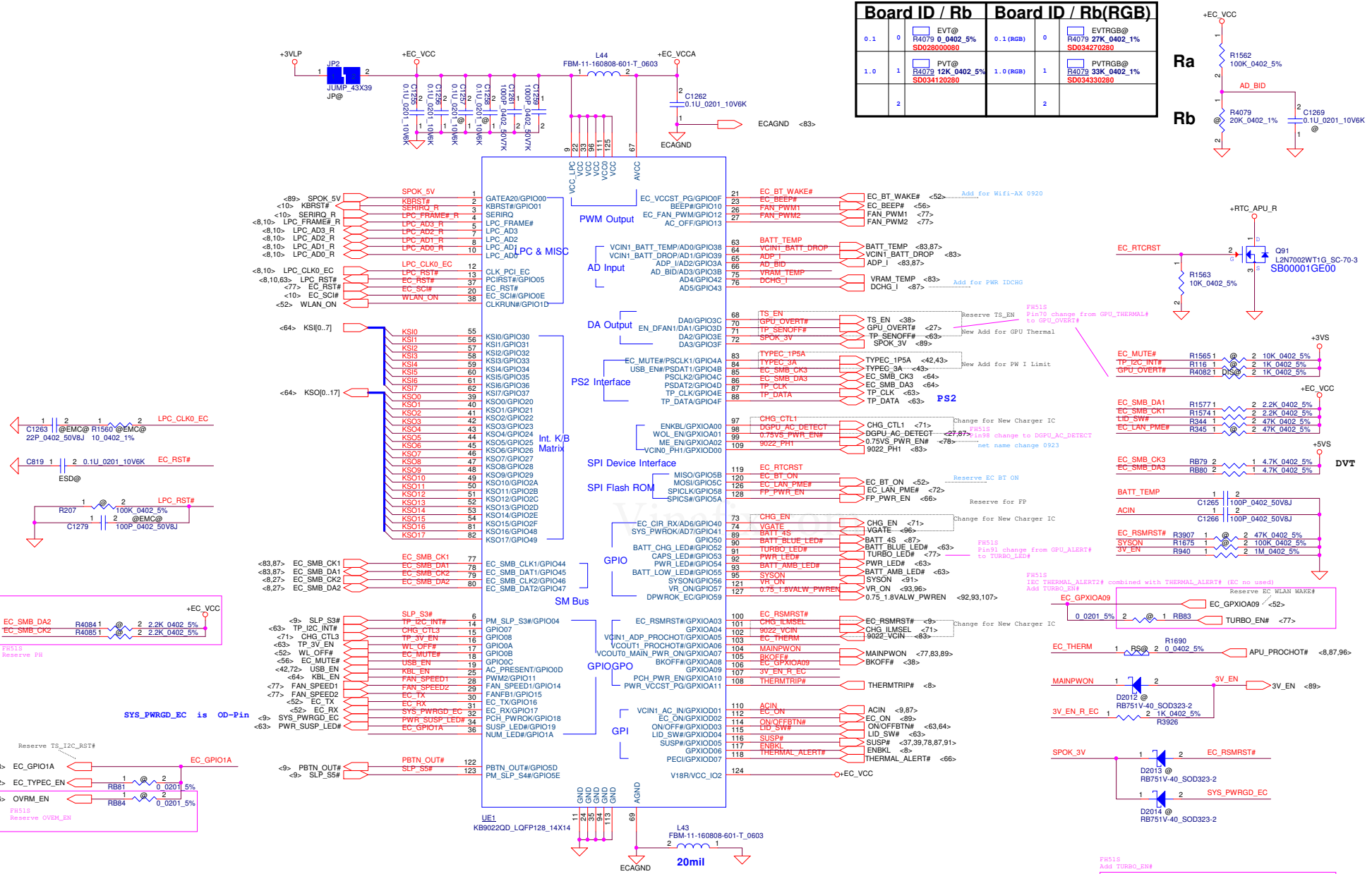


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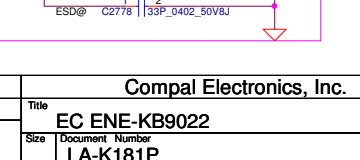
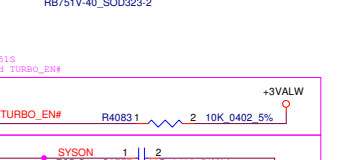
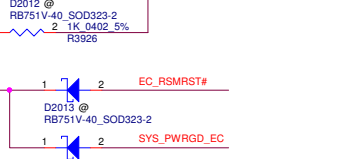
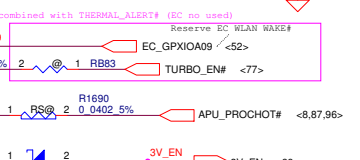
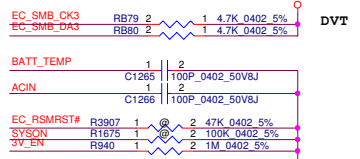
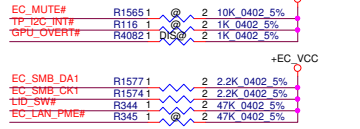
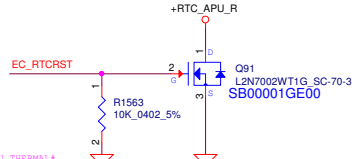
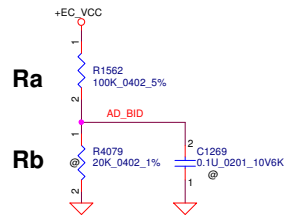
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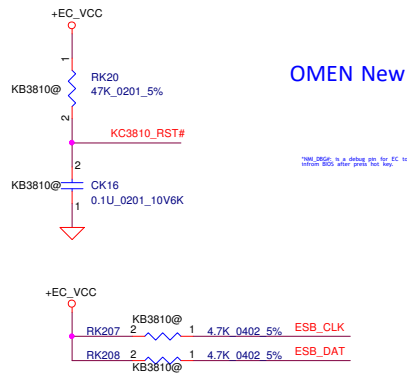


Board ID / Rb				Board ID / Rb(GB)			
0.1	0		EVT@ R4079 0.0402_5% SD028000080	0.1 (RGB)	0		EVT@ R4079 27K 0402_1% SD034270280
1.0	1		PVT@ R4079 12K 0402_5% SD034120280	1.0 (RGB)	1		PVT@ R4079 33K 0402_1% SD034330280
	2				2		



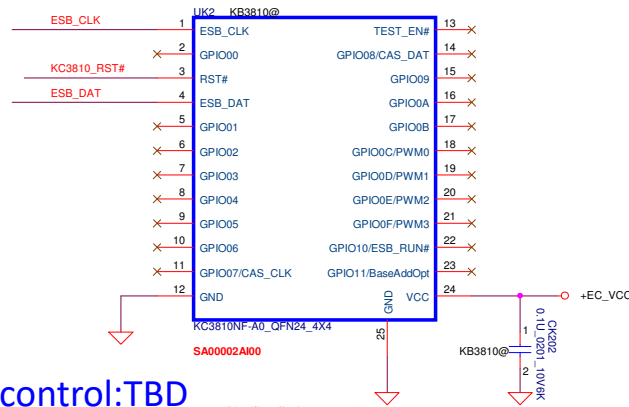
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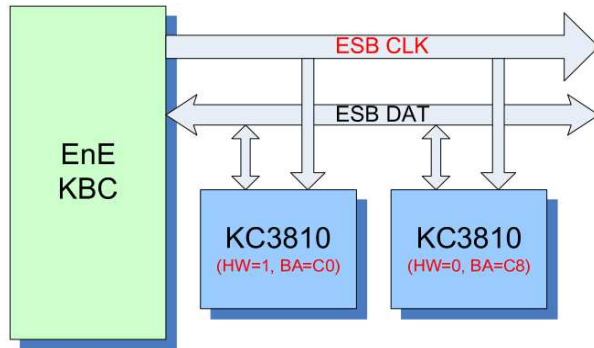
OMEN New ESB CLK&DAT for Extend I/O

No support on FH51S



- JEDEC 100-24-01 24 Pin QFN
1. USB_CTL1(GPIO4B Pin84)
 2. USB_CTL2(GPIO3F Pin72)
 3. USB_CTL3(GPIO1D Pin38)
 4. USB_CHARGE_EN(GPIO1A Pin36)
 5. GPU_OVERTH(GPIO0D Pin19) == DPFS0 NO USE
 6. LAN_PWR_EN(GPIO4D Pin6)
 7. WL_PWR_EN_EC(GPIO61 Pin98)
 8. DCDC1_EN(GPIO4B Pin72) == DPFS0 NO USE
 9. USB_ON#(GPIO37 Pin 121)
 10. LED : 5 Pin.

Some EC GPIO maybe change to extend IO control:TBD



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Date: Wednesday, April 08, 2020		Sheet 61 of 116			

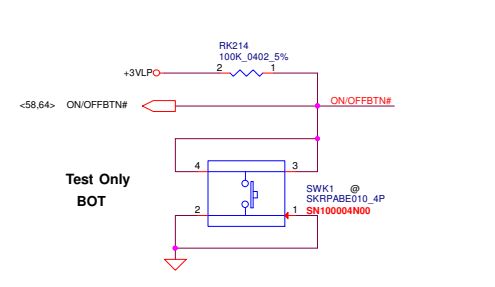
Reserve

Vinafix.com

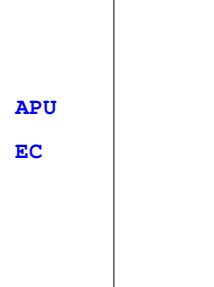
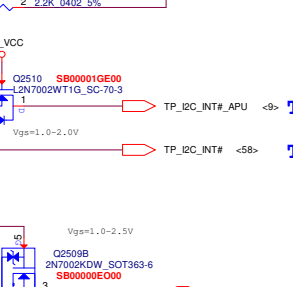
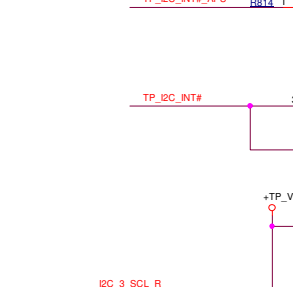
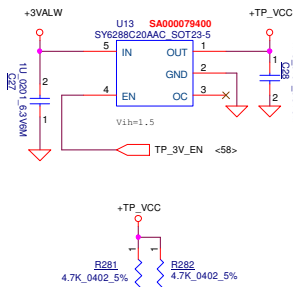
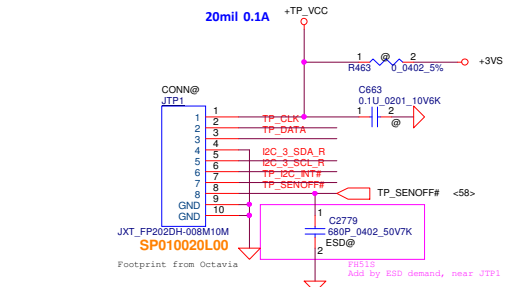
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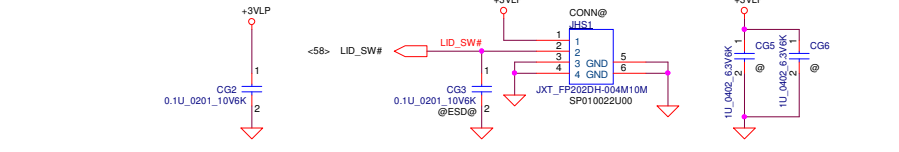
ON/OFF BTN



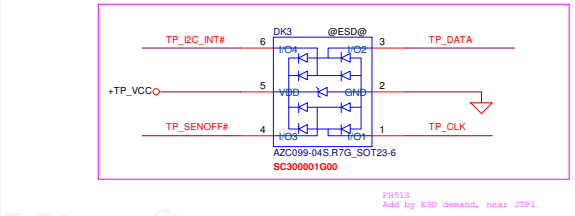
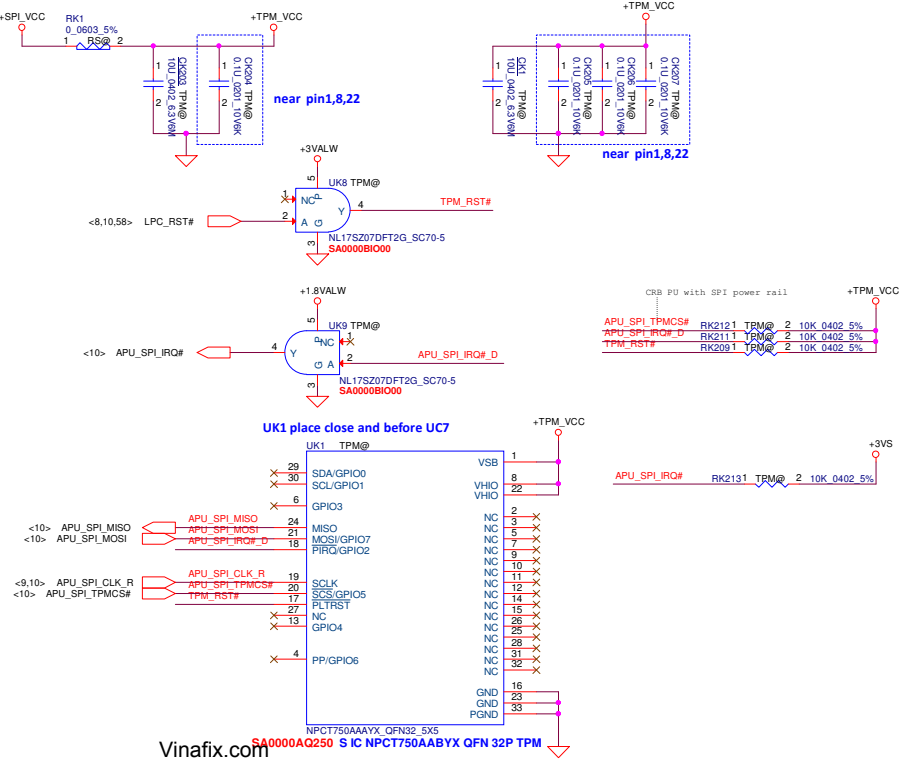
TP/B Conn.



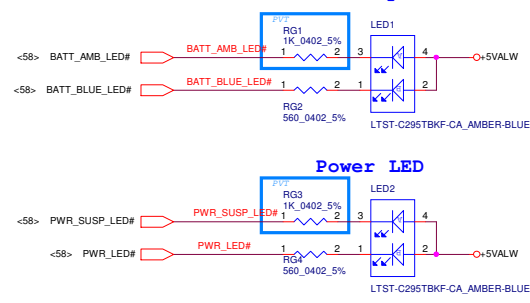
Lid Switch (Hall Effect Switch)



TPM

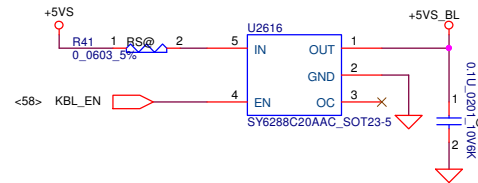


LED

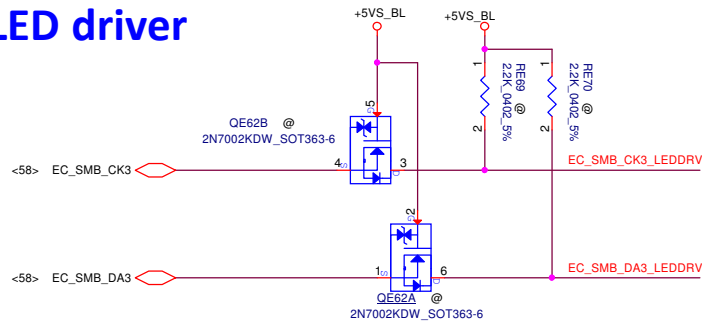


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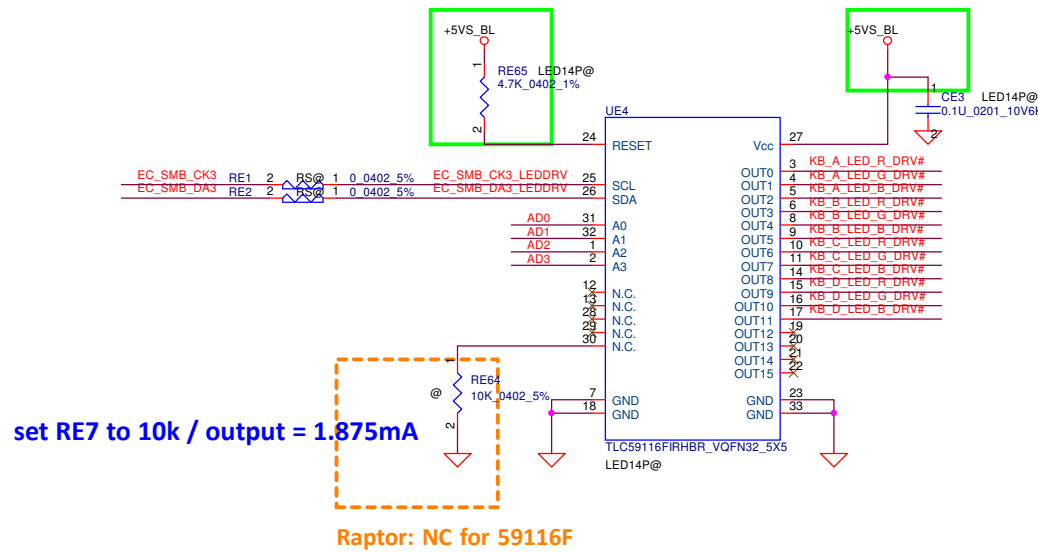
KB BackLight



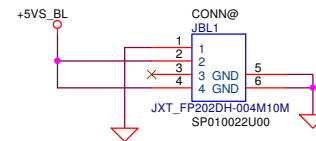
LED driver



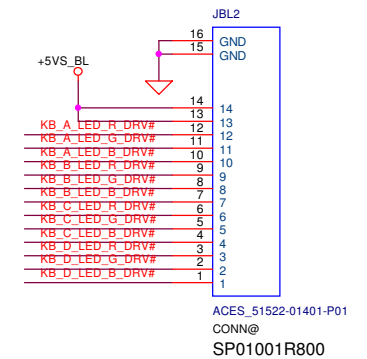
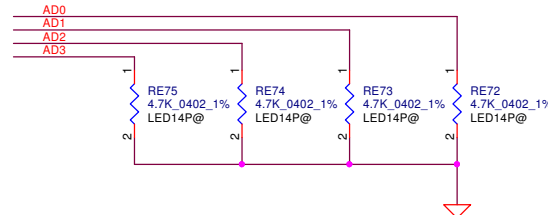
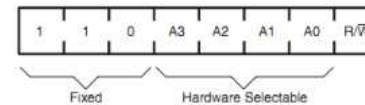
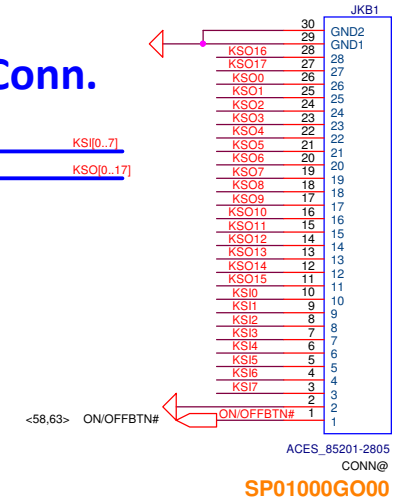
Vinafix.com



KB Conn.



<58> KS[0..7] KS[0..7]
<58> KSQ[0..17] KSQ[0..17]



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								KB/Backlight/RGB							
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Reserve

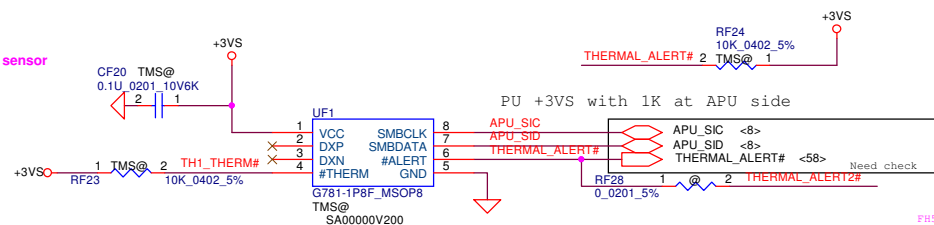
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THERMAL SENSOR

FH51S
A+N w/o STT, change thermal sensor



Slave Address

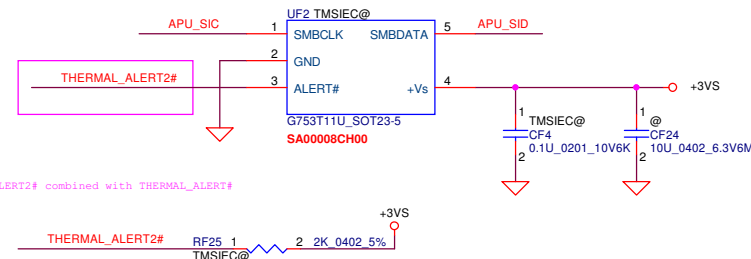
The G781 appears to the SMBus as one device having a common address for both ADC channels.

The G781 and G781-1 have the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G781	1	0	0	1	1	0	0
G781-1	1	0	0	1	1	0	1

SMBUS ADDRESS
1001_101xb

THERMAL IEC



FH51S
IEC THERMAL_ALERT2# combined with THERMAL_ALERT#

The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

The G753 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

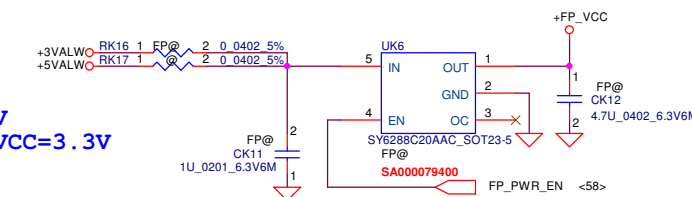
ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

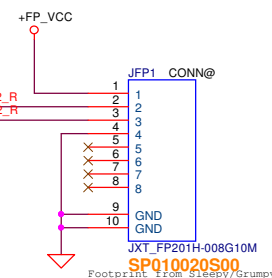
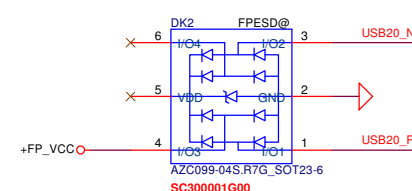
Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



JFP1

PIN	SA464K-2200
1	+FP_VCC (3V)
2	D+
3	D-
4	GND
5	NC
6	NC
7	NC
8	NC



Footprint from Sleepy/grumpy

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								Thermal sensor			
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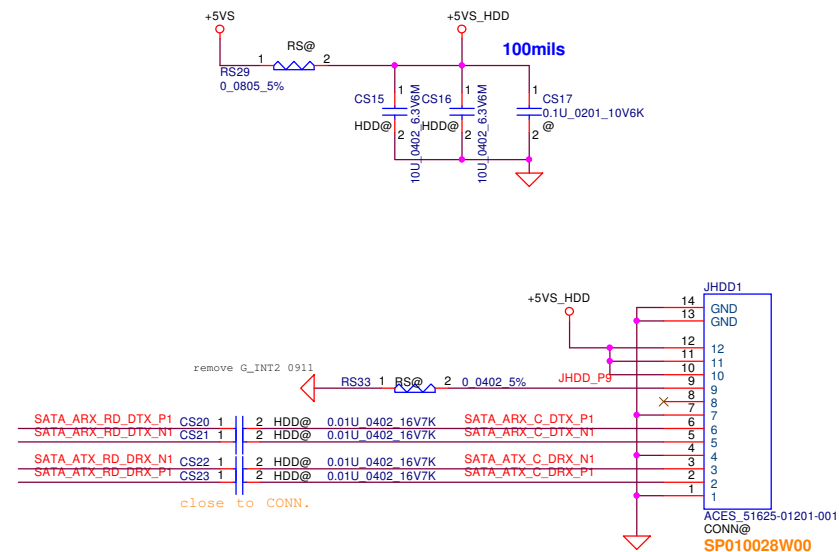
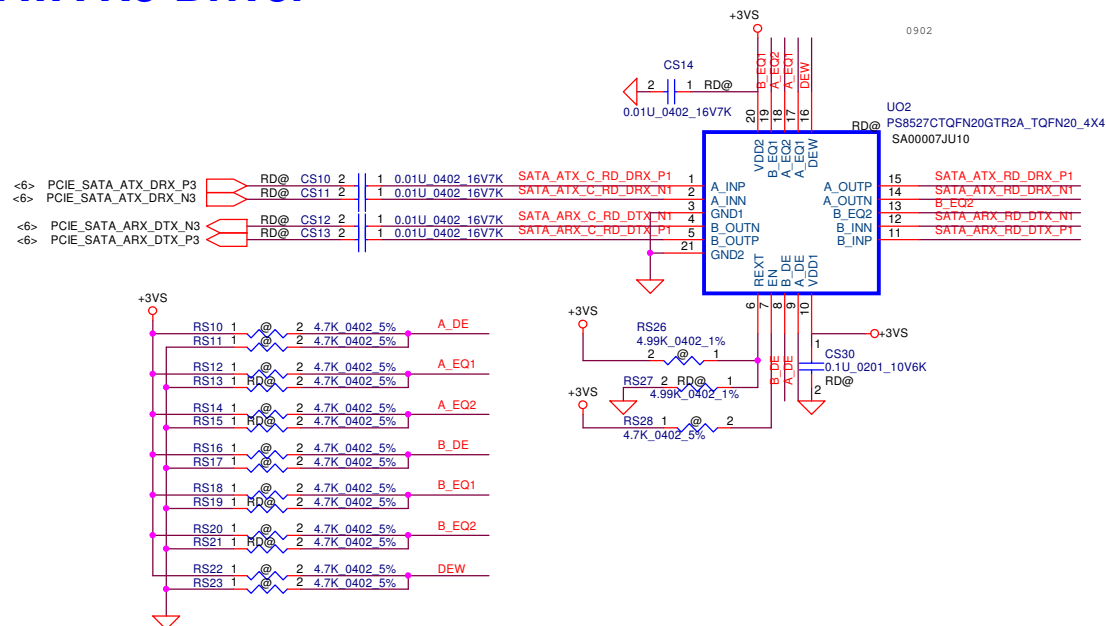
Reserve

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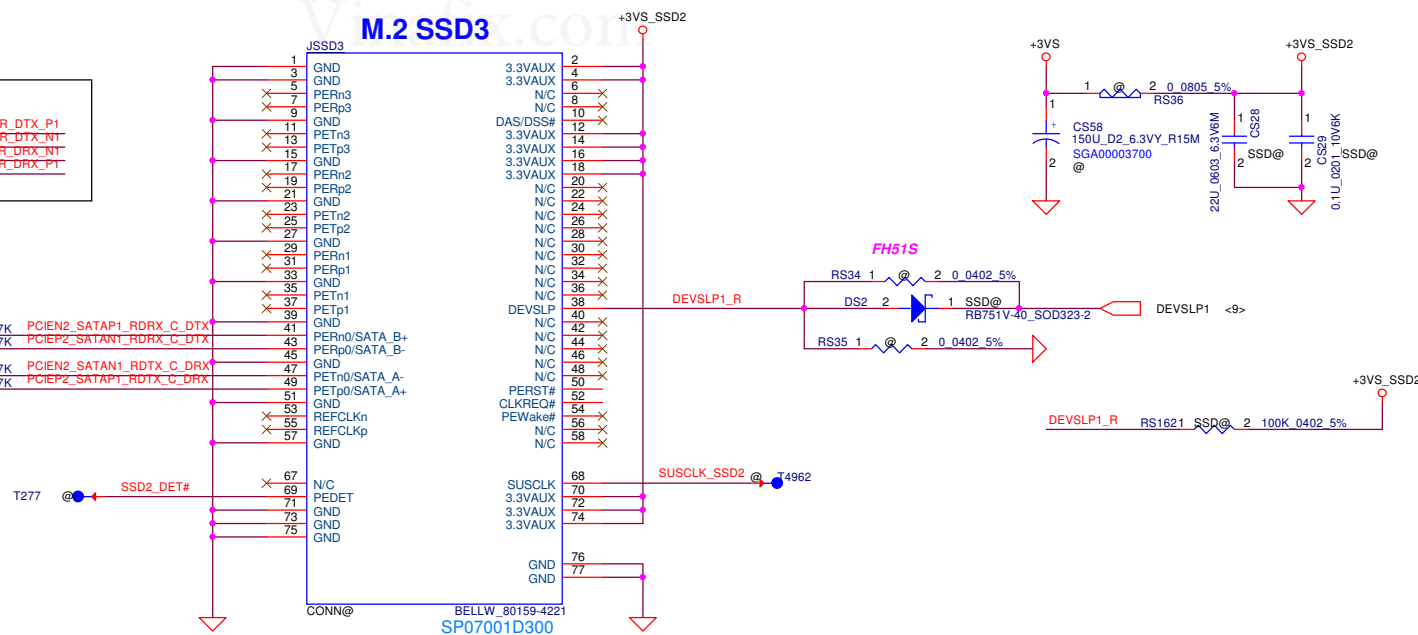
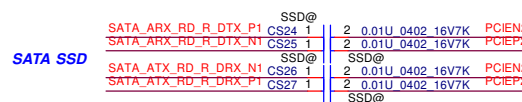
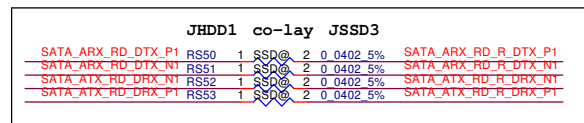
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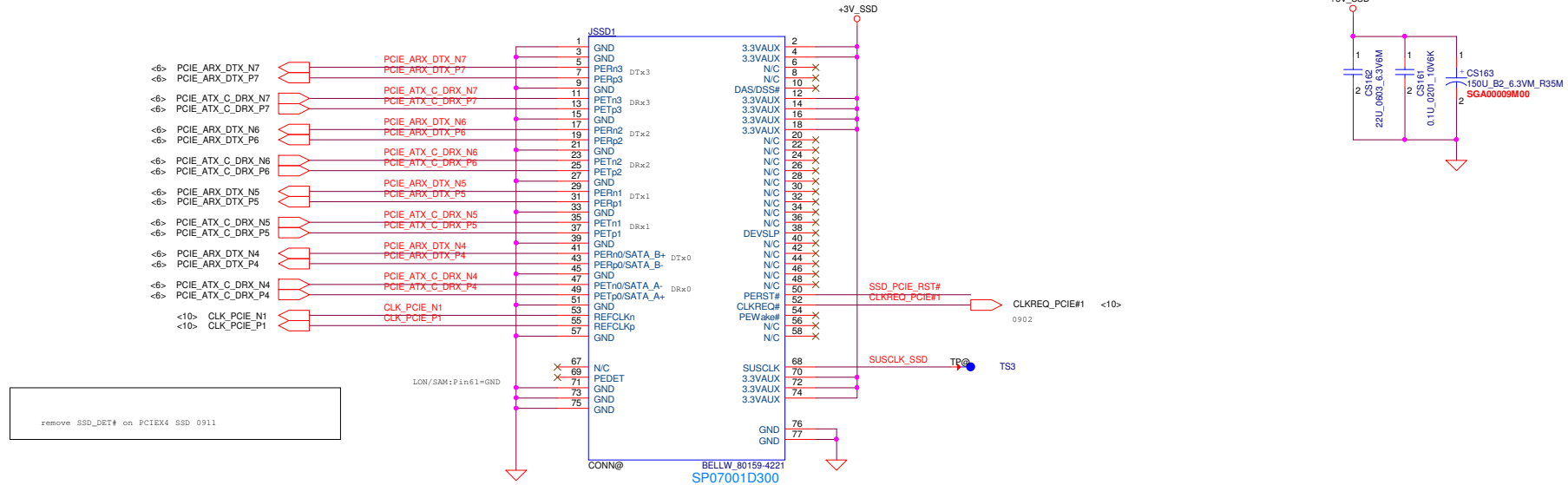
SATA Re-Driver



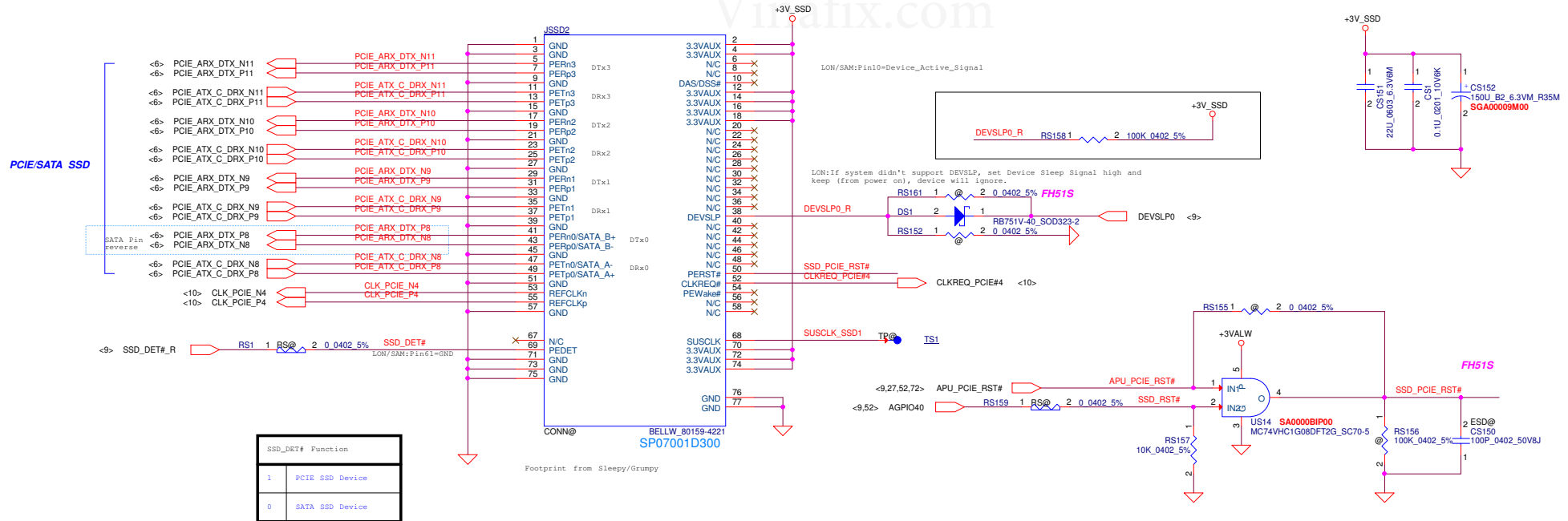
M.2 SSD3



PCIEx4 NGFF SSD Conn.



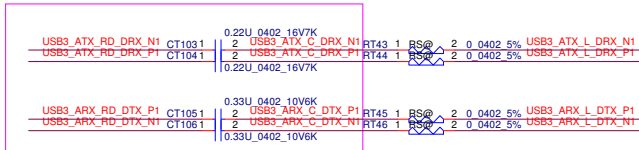
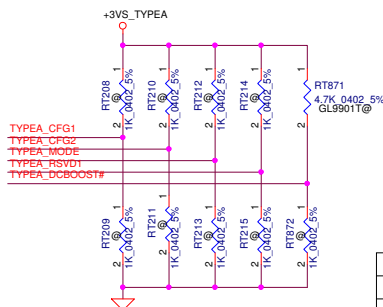
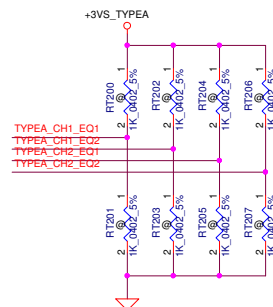
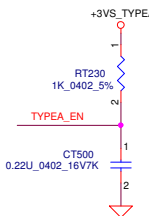
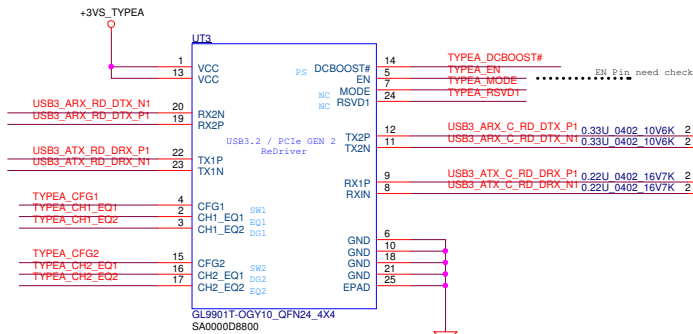
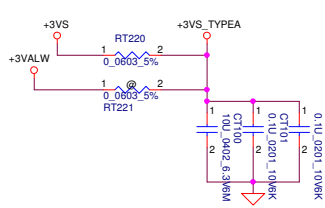
PCIE/SATA NGFF SSD Conn.



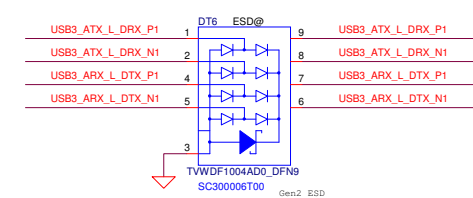
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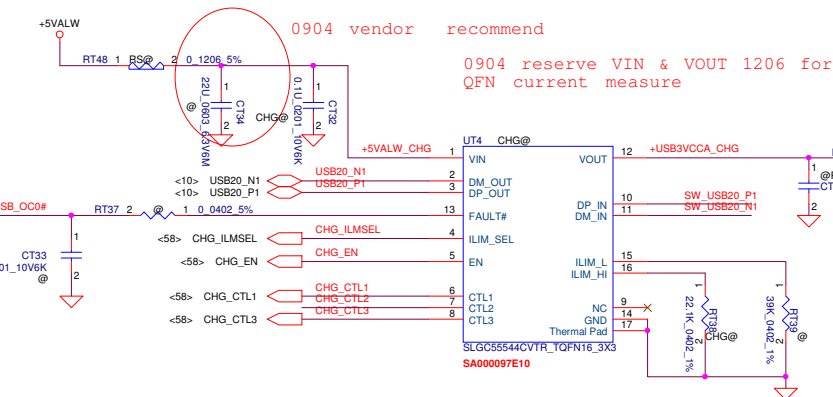
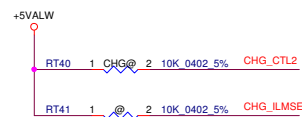
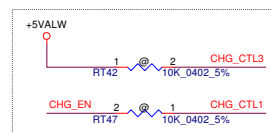
2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H



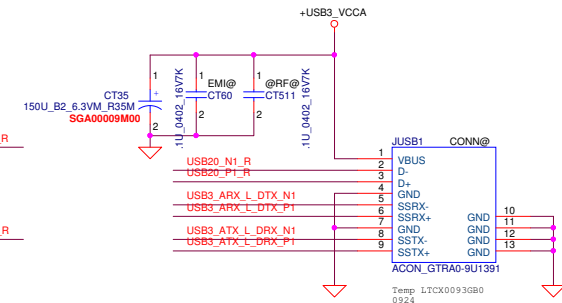
USB Host Charger Truth Table

CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	SDP1	ILIM_H	Data Lines Connected
1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	CDP	ILIM_H	Data Lines Connected

CHG_EN	CTL1
0	0
1	0
1	0
1	1

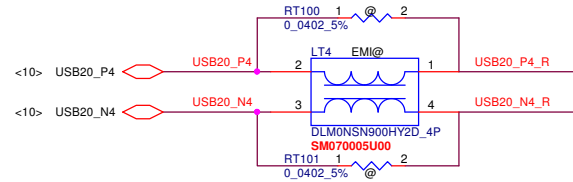


USB3.0 Conn.

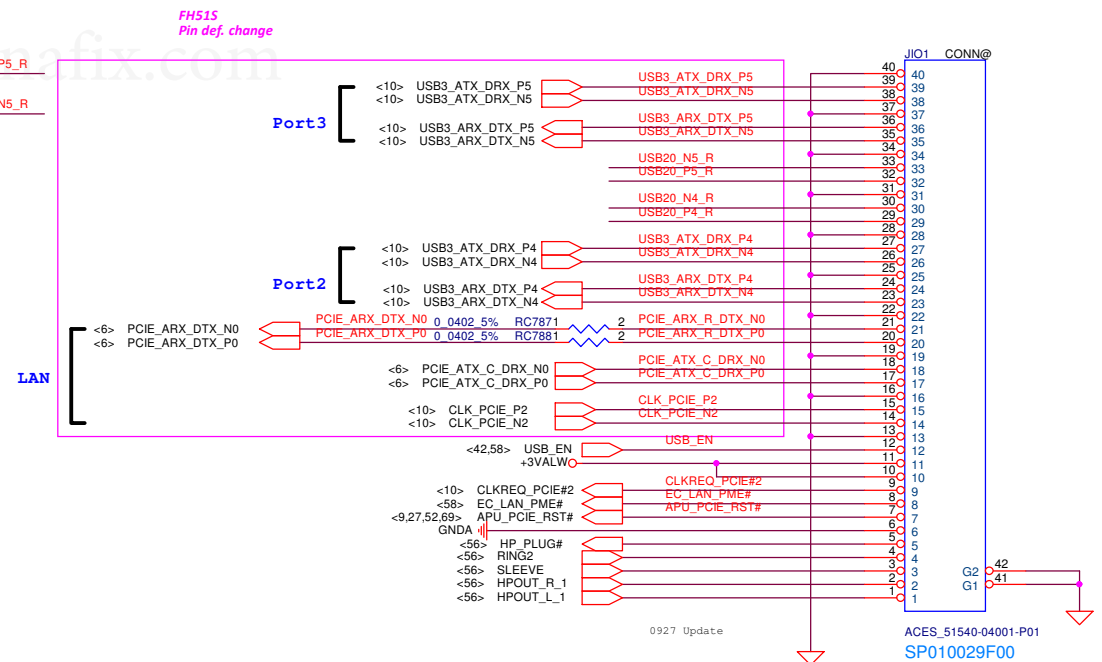
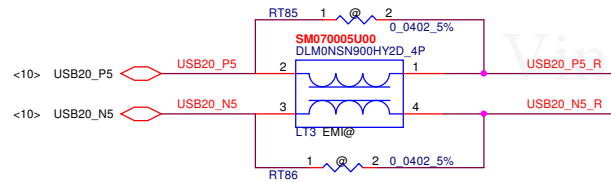


ILM R vaule
 Ios (mA) = 50250/R (Kohm)
 ILIM_Hi = 2273mA
 ILIM_L = 1288mA

USB3.0 (Port 2)



USB3.0 (Port 3)



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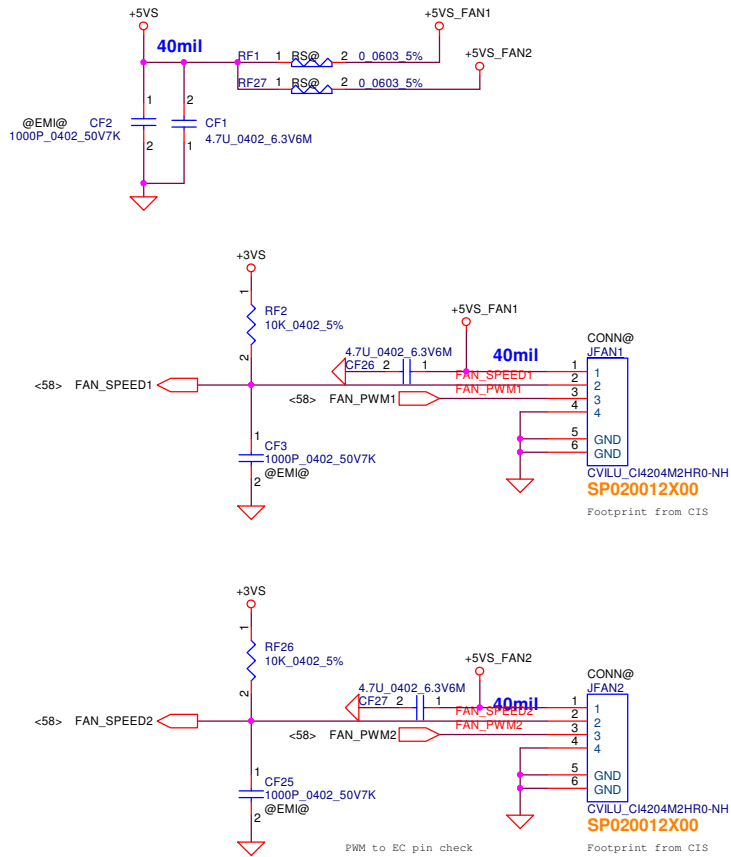
Reserve

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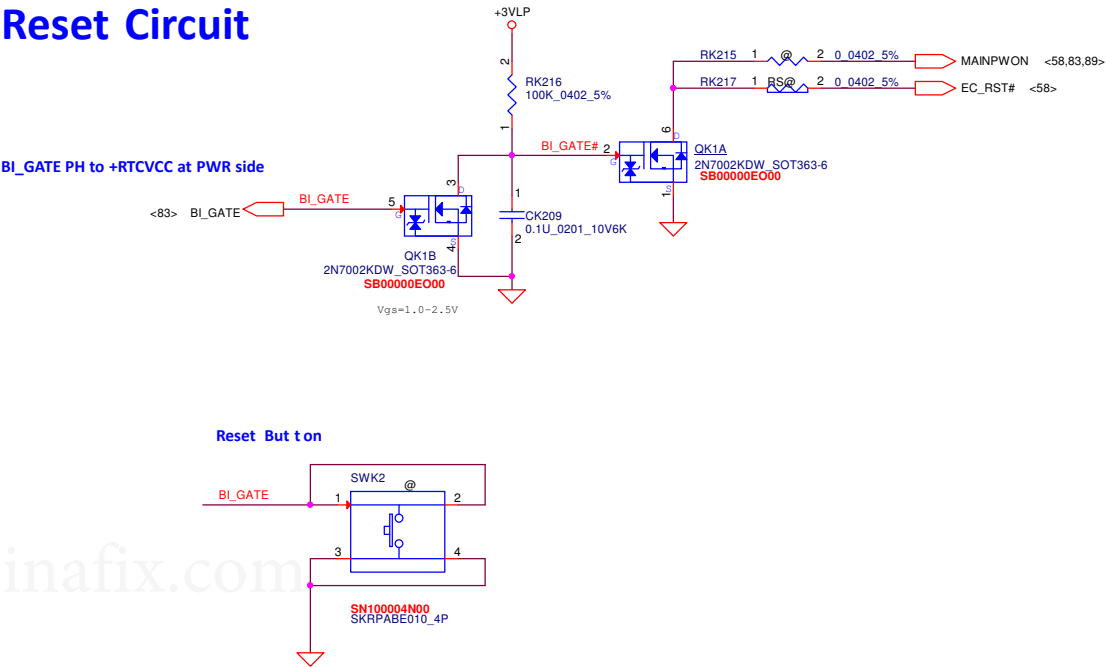
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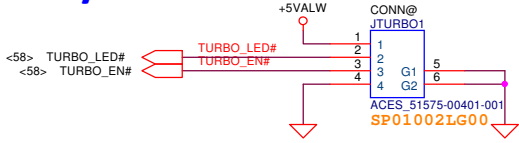
FAN Conn



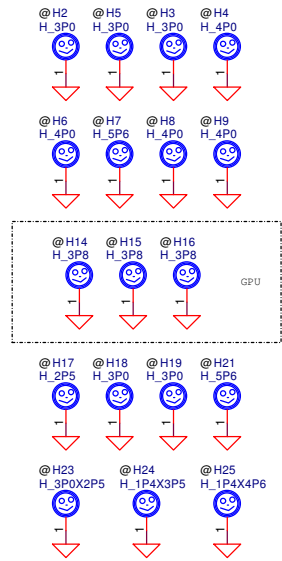
Reset Circuit



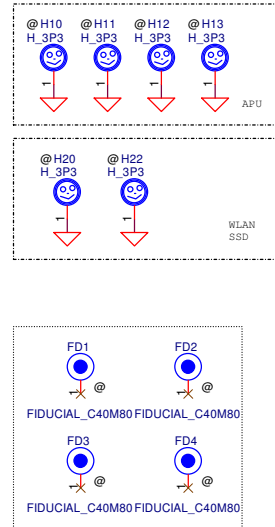
Turbo Key



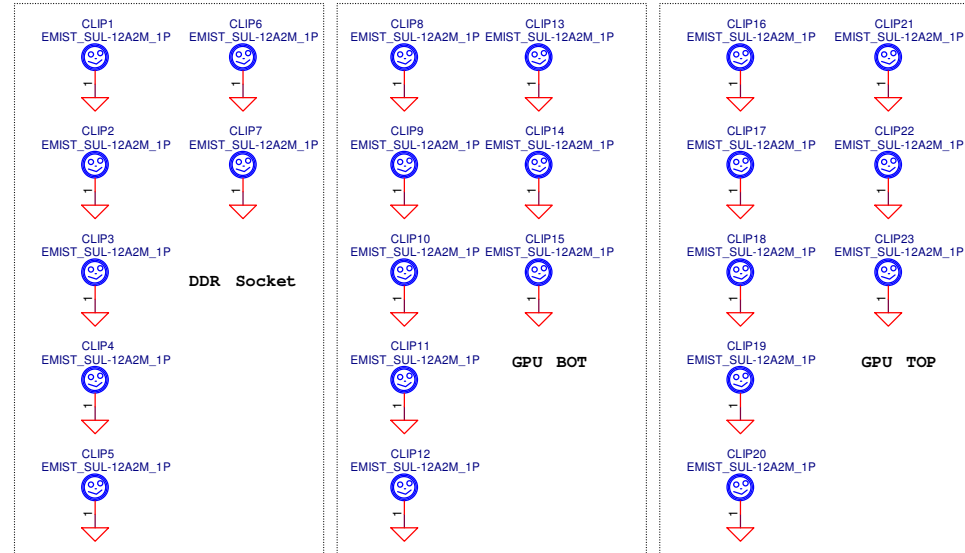
Screw Hole



Stand OFF



CLIP



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ROYALTY HDMI W/LOGO+HDCP
RO0000003HM

ZZZ DAZ10@



PCB FH51S LA-K181P LS-J881P/J872P
DAZ32500100

ZZZ DA10@



PCB FH51S LA-K181P LS-J881P/J872P
DAA000N1010

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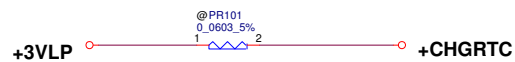
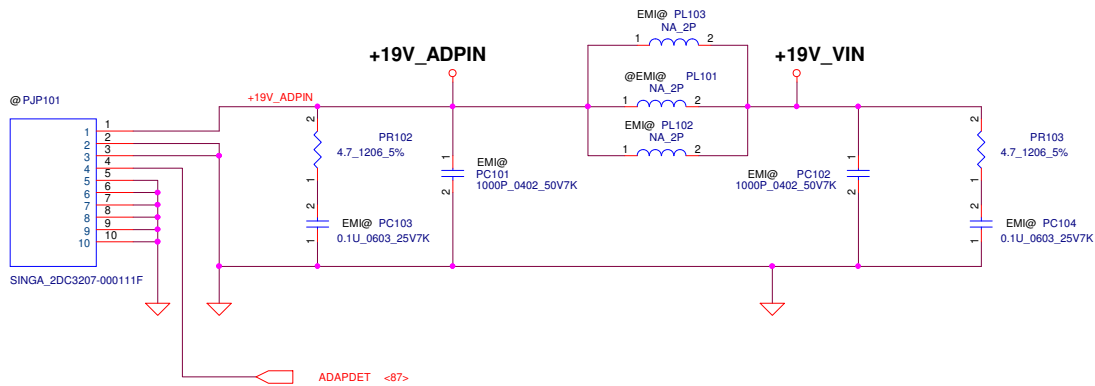
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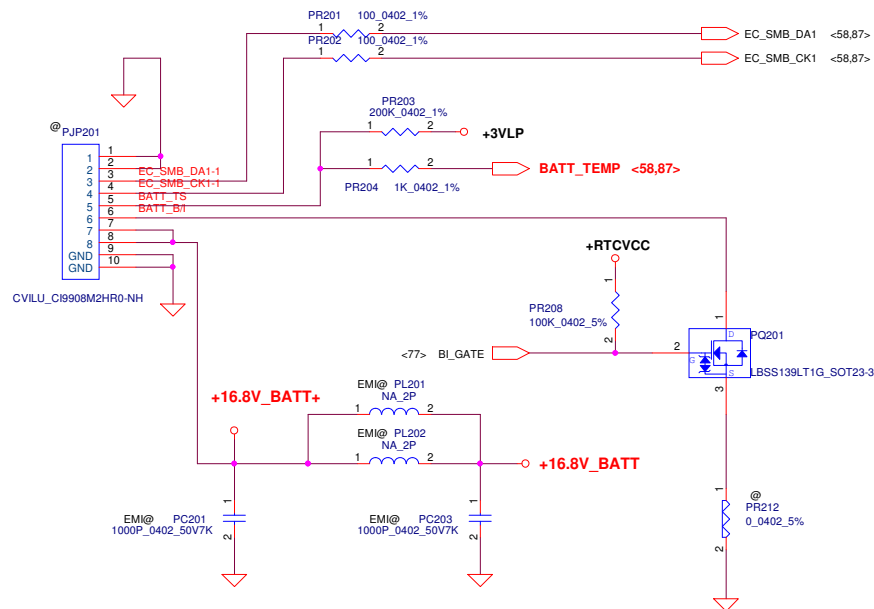
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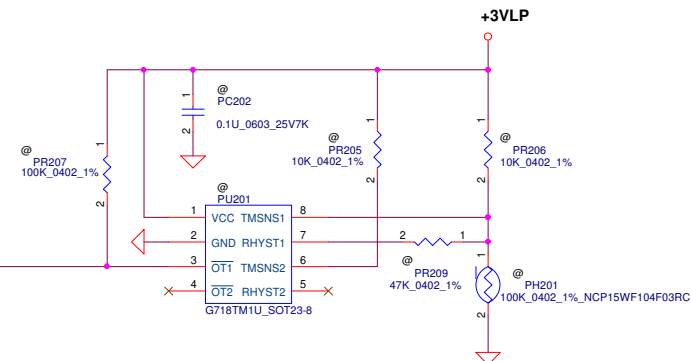
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<58,77,89> MAINPWON



For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

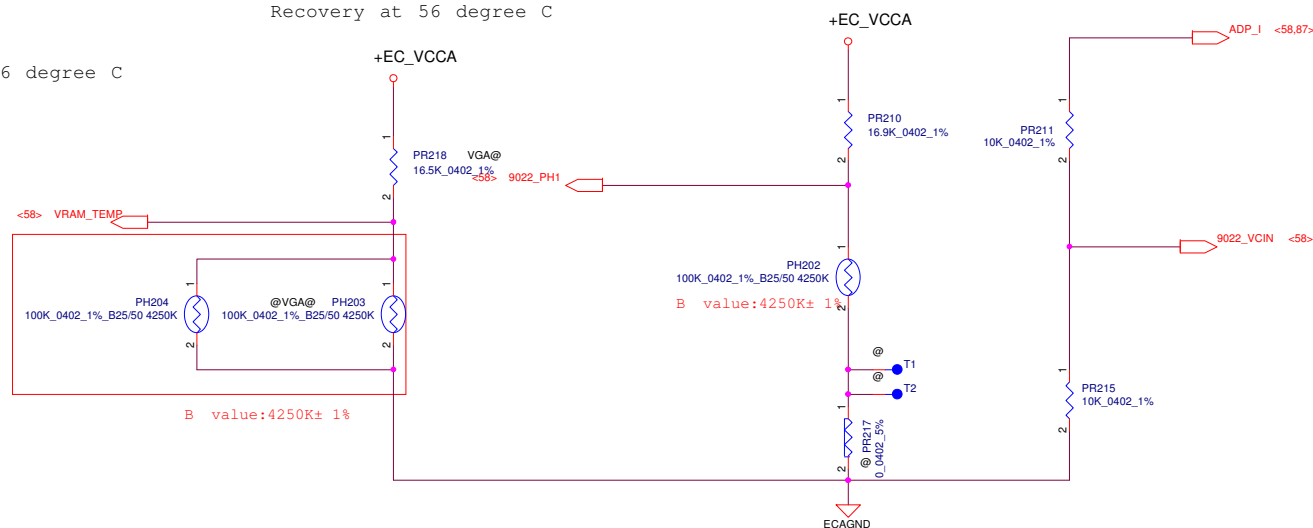
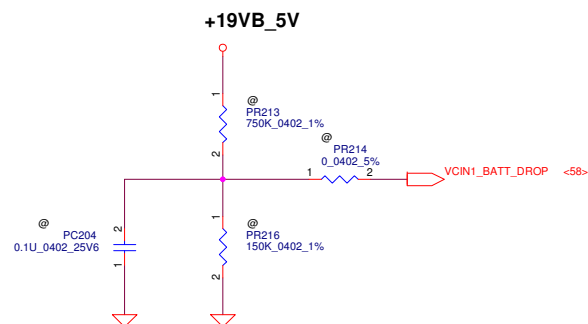
For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

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PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C

2013/10/02
Add for ENE9022 Battery Voltage drop detection. Recovery at 56 degree C
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



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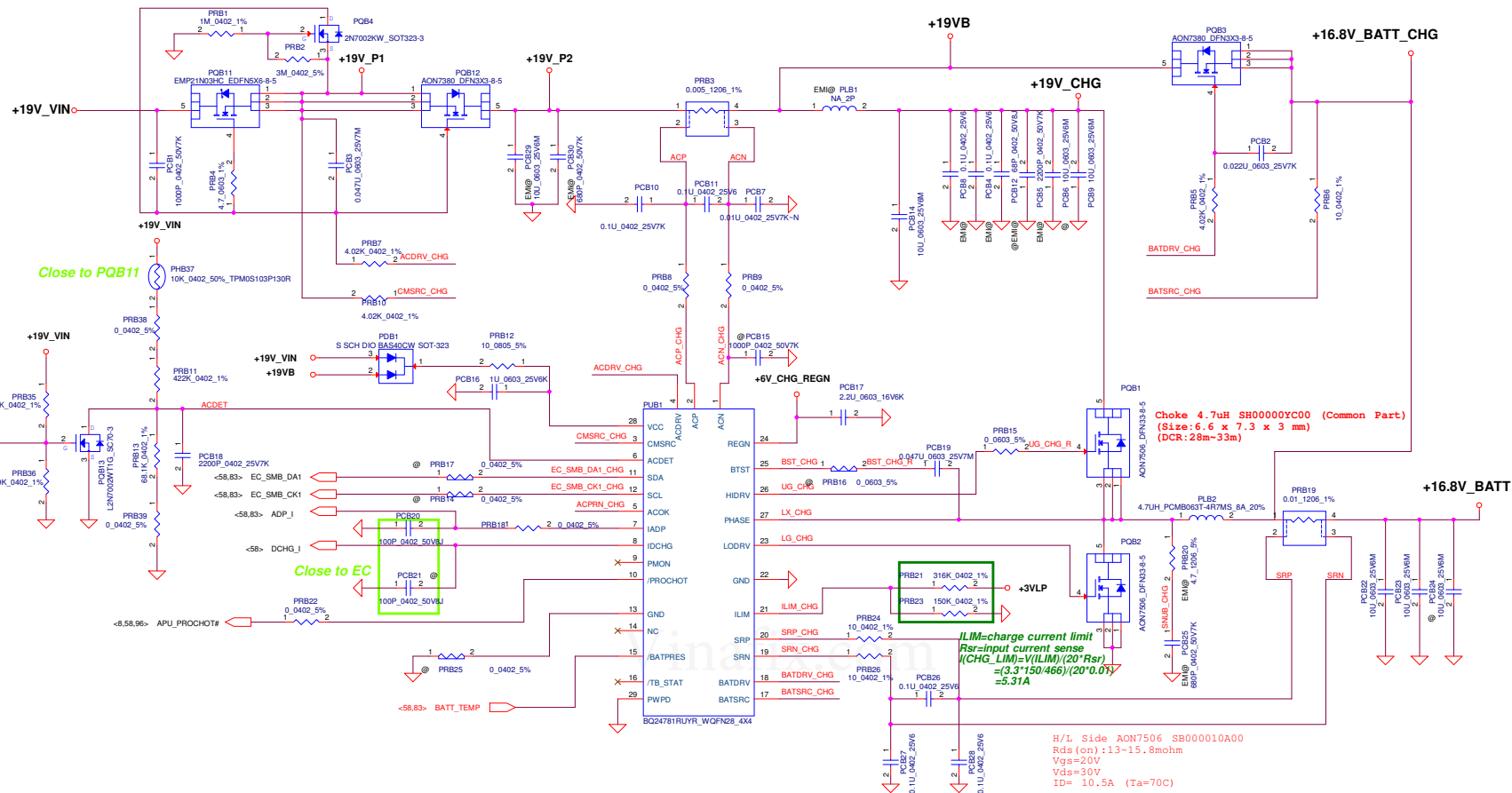
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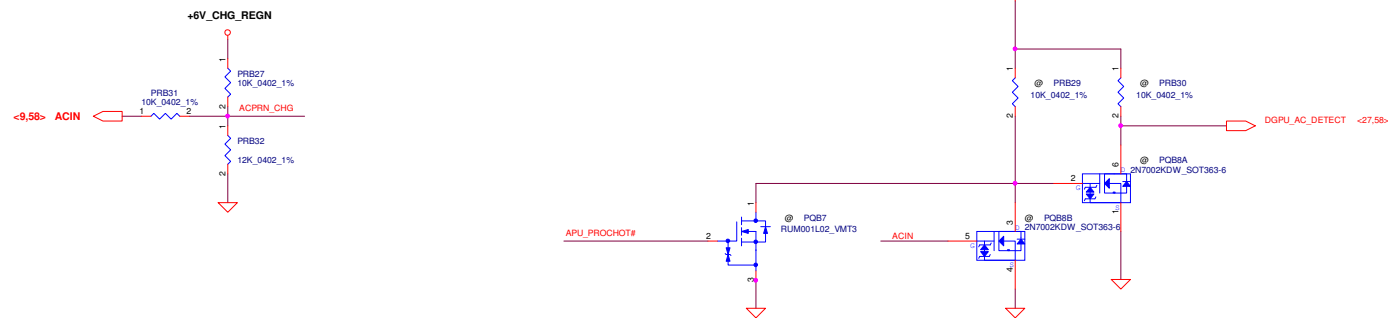
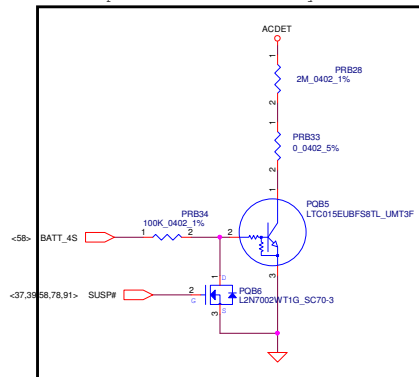
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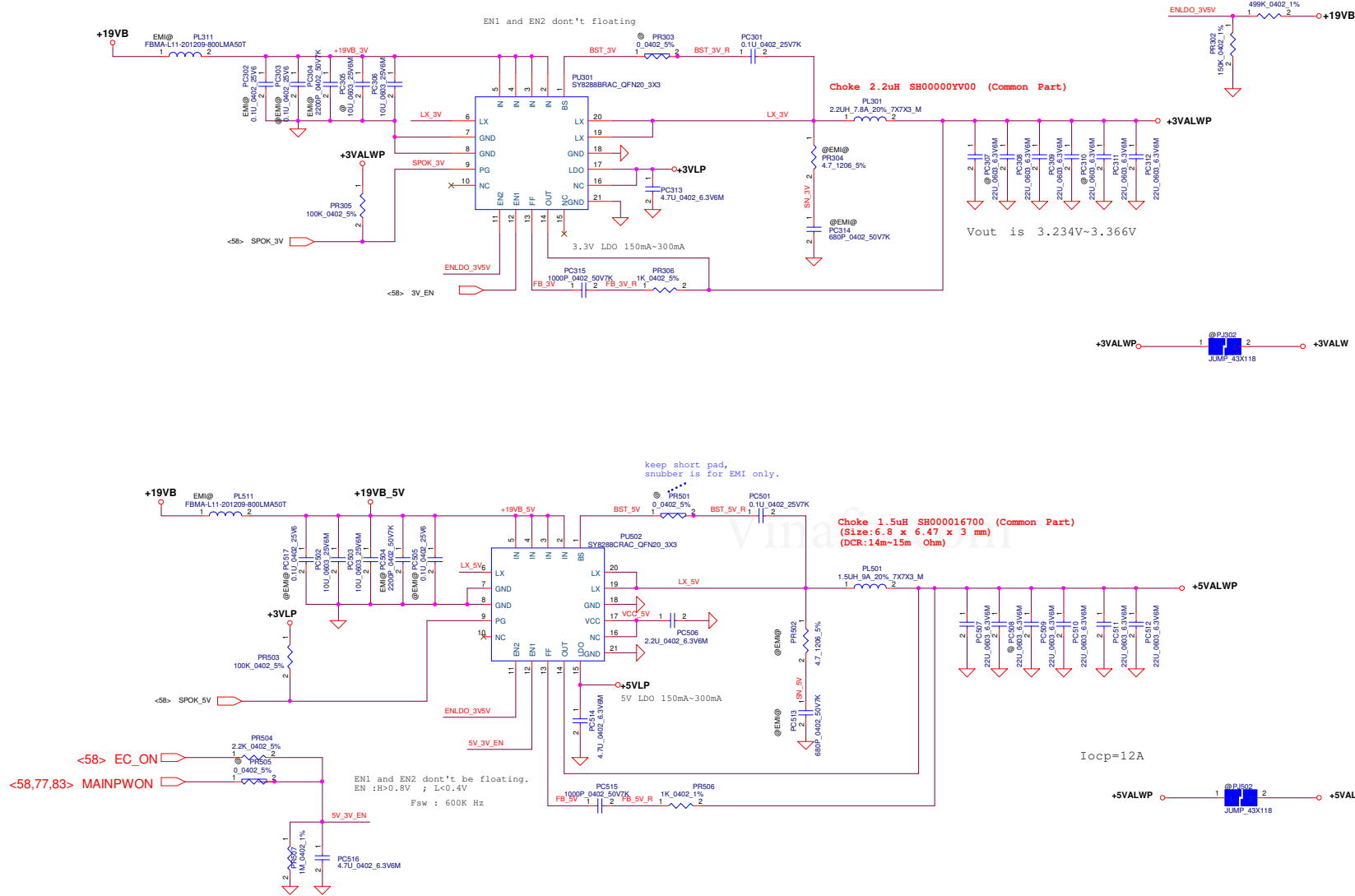
For 4S per cell 4.35V battery



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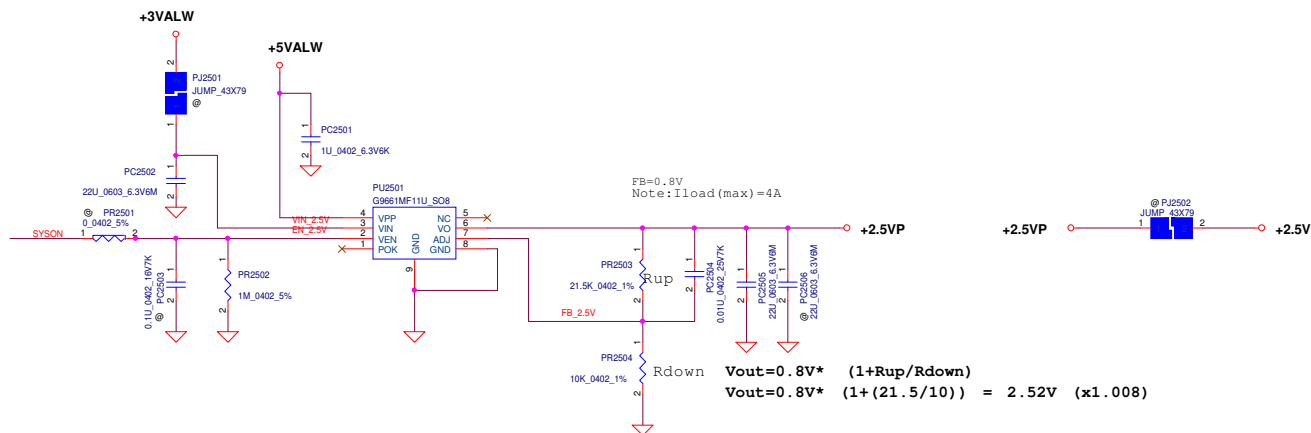
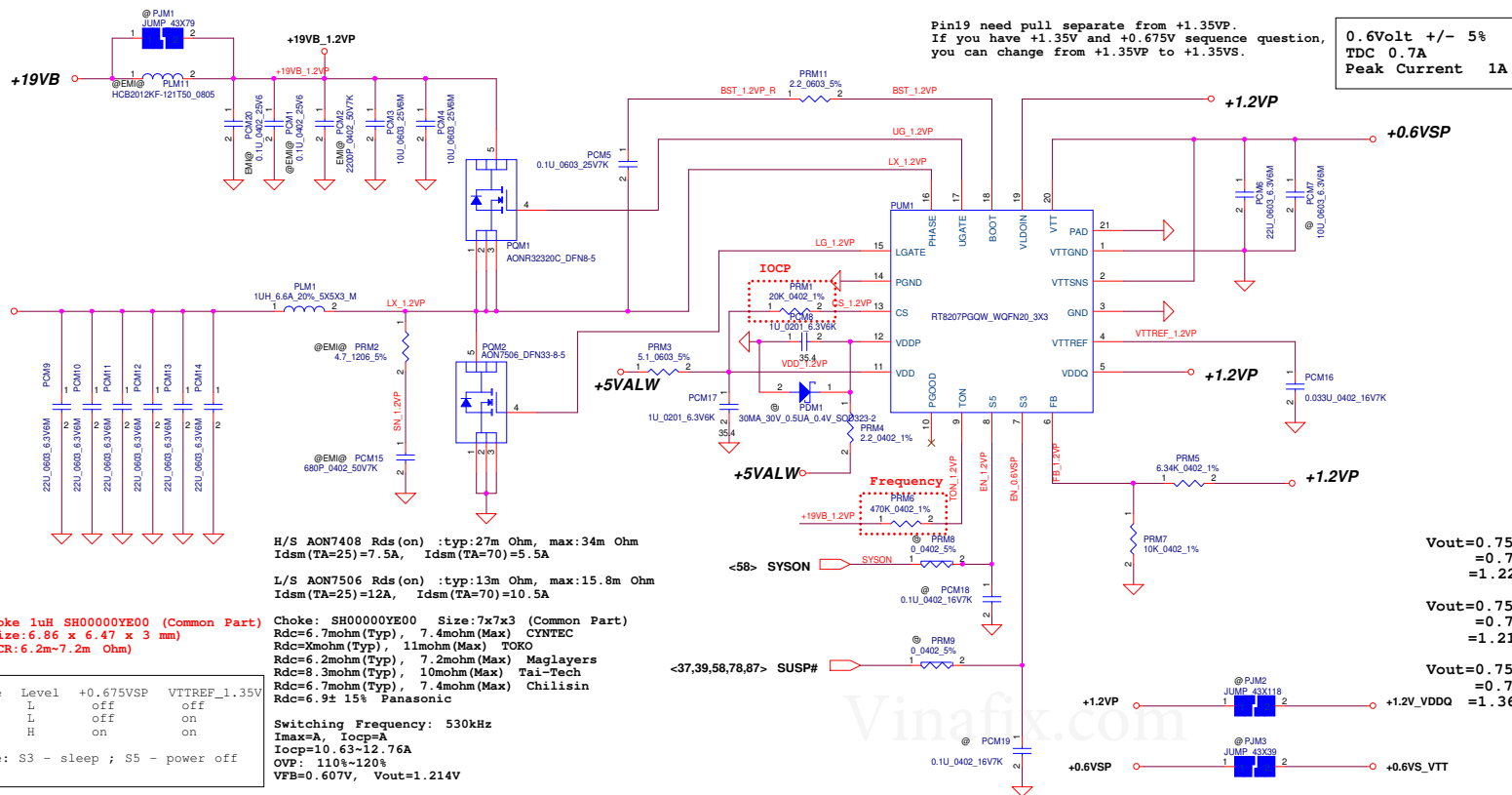
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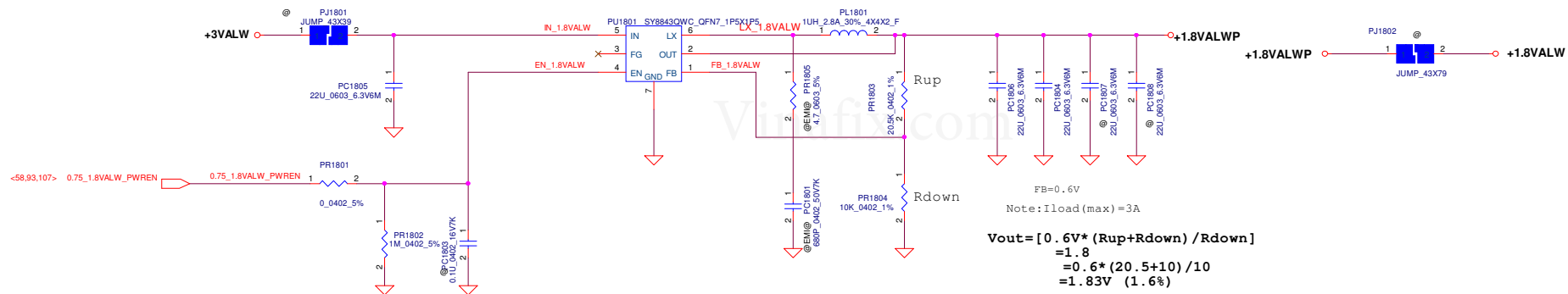


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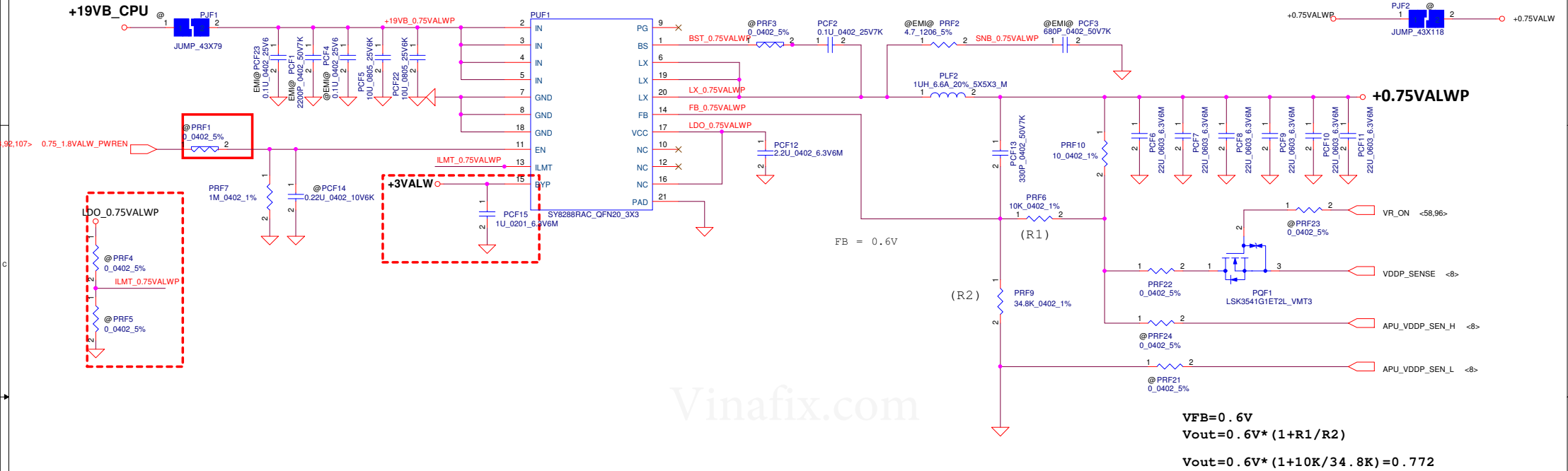
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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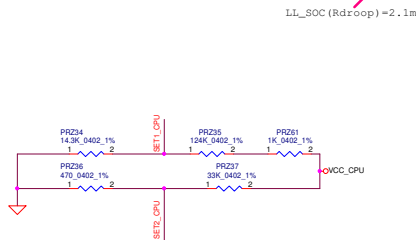
$I_{ocp_spike} = (3.19375 - 0.64) * PR755 / (2 * DCR * R_{imona})$
 I_{ocp_TDC} has relation between ocp_spike and ΔV_{SET1}
 $\Delta V_{SET1} = +5V5 * (PR788 / PR784)$

SVD_CPU and SVC_CPU RC filter put CPU side.
 SVT_CPU RC filter put controller side.

SVD and SVC RC filter put CPU side.
 SVT RC filter put controller side.



$I_{ocp_spike} = (3.19375 - 0.64) * PR709 / (DCR * R_{imona})$
 I_{ocp_TDC} has relation between ocp_spike and ΔV_{SET1}
 $\Delta V_{SET1} = +5V5 * (PR788 / PR784)$



LL_SOC (Rdriop) = 2.1m

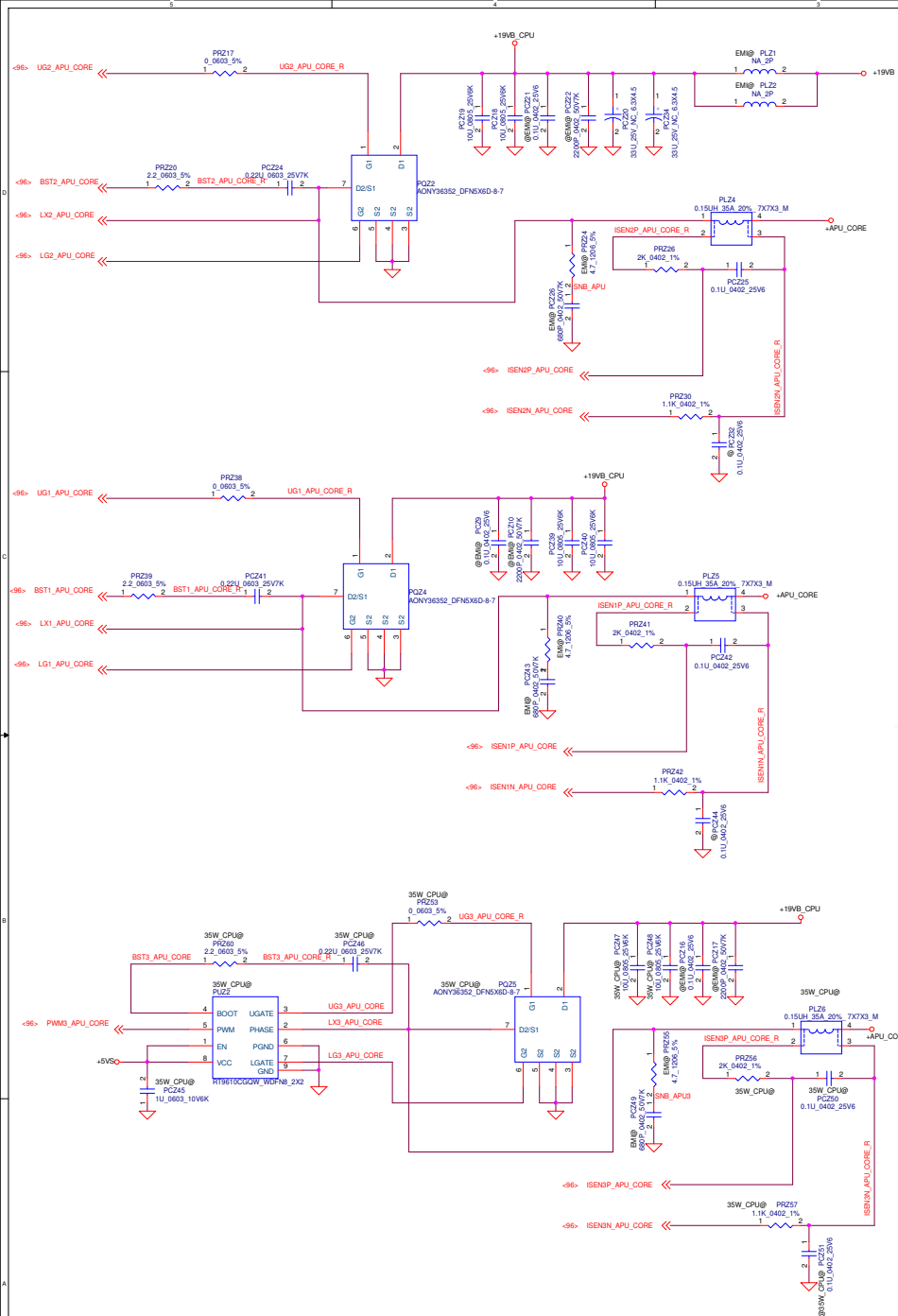
Pull high at HW side

Confirm SW side the pull high resistor

EN: high > 2V, Low < 0.8V
 Can't be floating.

V_{core}
 $L=0.15\mu H$, $DCR=0.9m\Omega$, $LL=0.7m\Omega$, $OCF=135A$
 V_{core_NB}
 $L=0.15\mu H$, $DCR=0.9m\Omega$, $LL=2.1m\Omega$, $OCF=30A$

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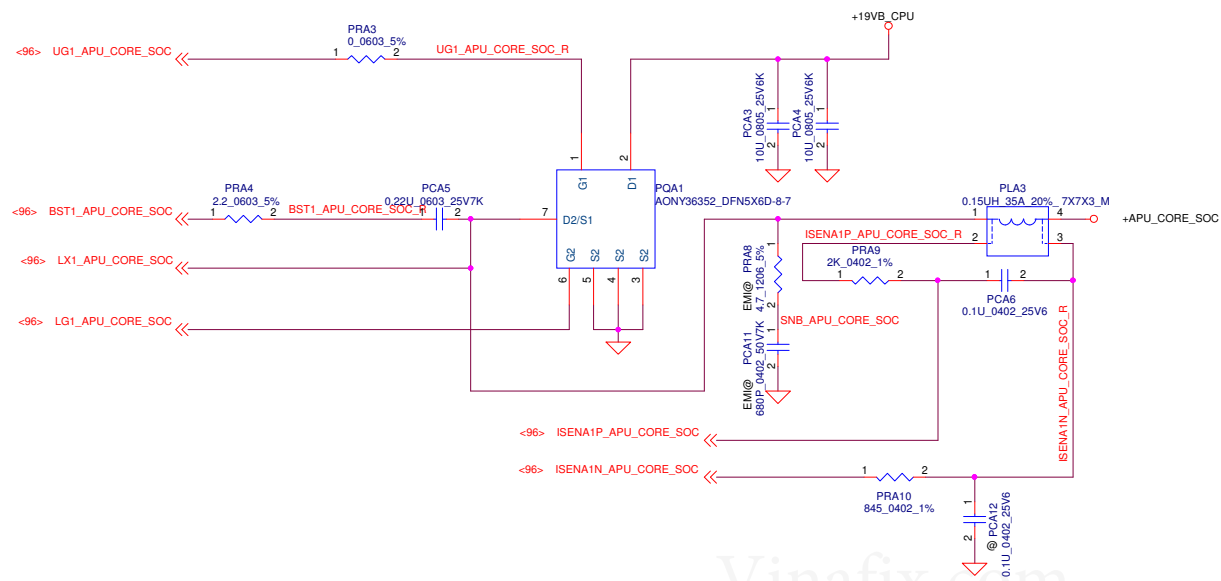


APU_core
 TDC 35A (15W & 25W), 56A (35W)
 EDC 45A (15W & 25W), 70A (35W)
 OCP current 63A (15W & 25W), 98A (35W)
 Load line -0.7mV/A
 FSW=430kHz
 DCR 0.98mohm +/-5%
 TYP MAX
 H/S Rds(on) :11.7mohm , 14mohm
 L/S Rds(on) :2.7mohm , 3.3mohm

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+APU_CORE_SOC
TDC 10A (15W & 25W & 35W)
EDC 13A (15W & 25W & 35W)
OCP current 24.2A (15W & 25W & 35W)
Load line -2.1mV/A
FSW=400kHz
DCR 0.98mohm +/-5%
TYP MAX
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

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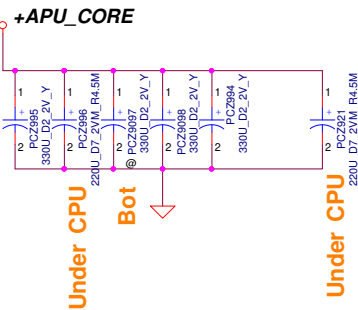
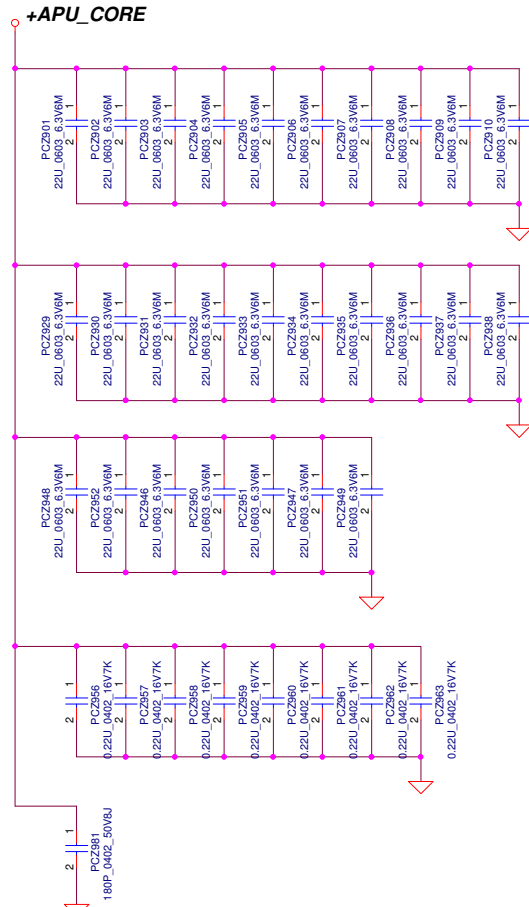
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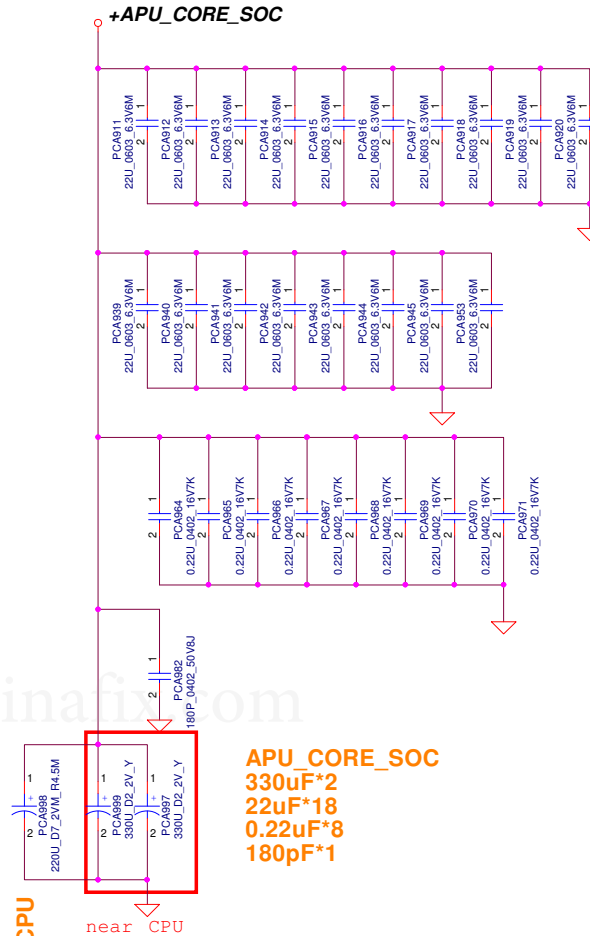
+APU_CORE



APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

330u is common part SGA00009S00

+APU_CORE_SOC



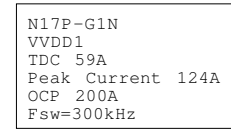
APU_CORE_SOC
330uF*2
22uF*18
0.22uF*8
180pF*1

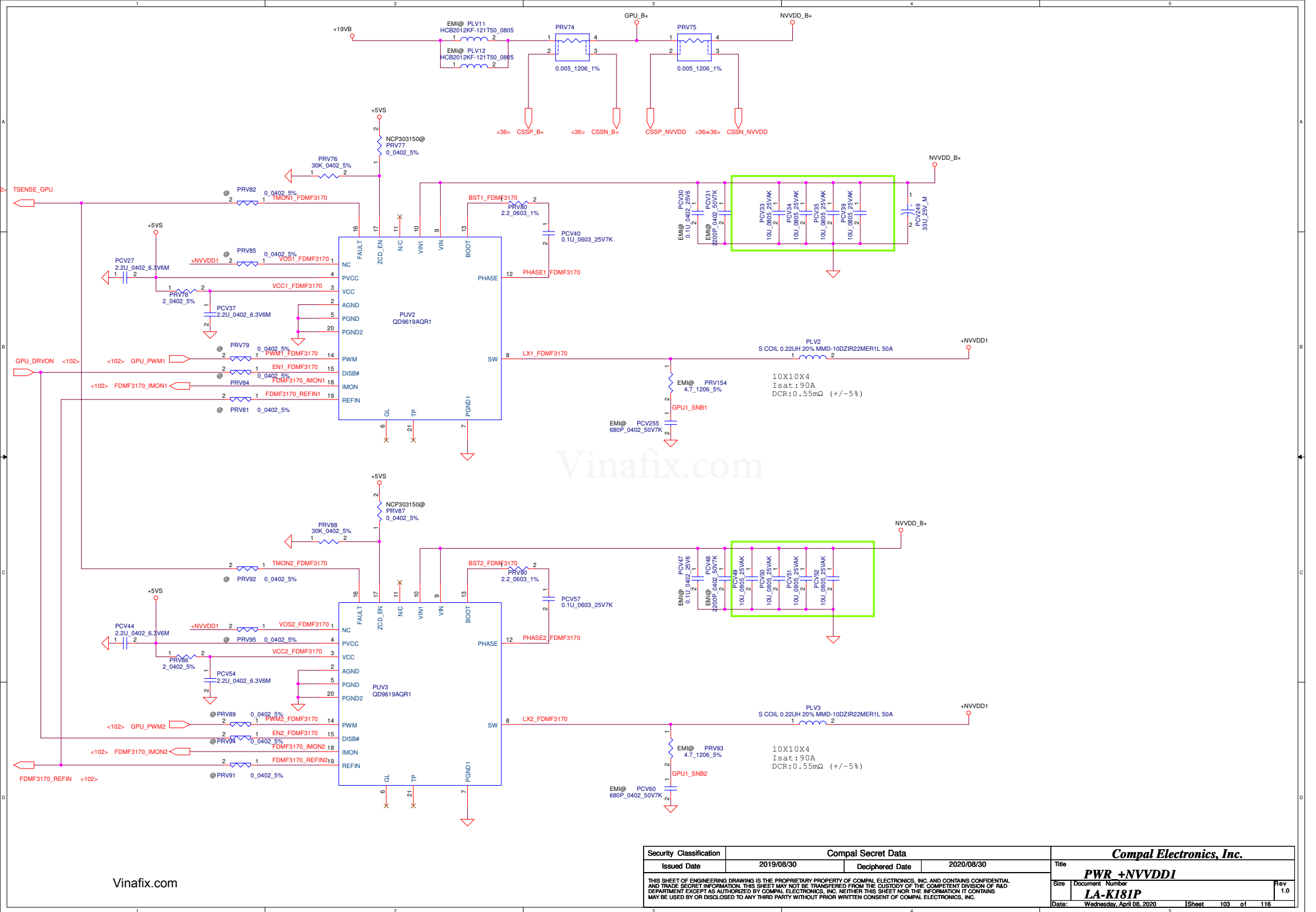
330u is common part SGA00009S00

Under CPU

near CPU

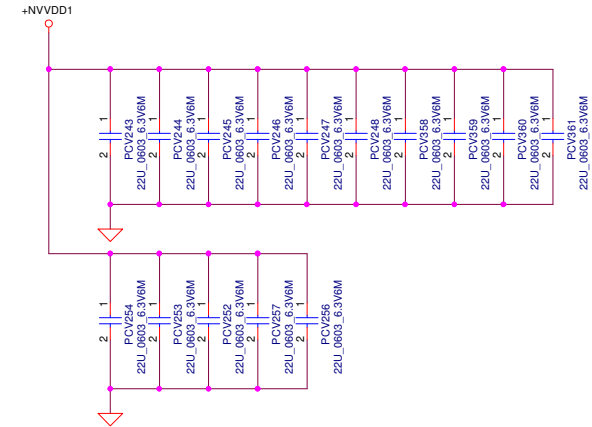
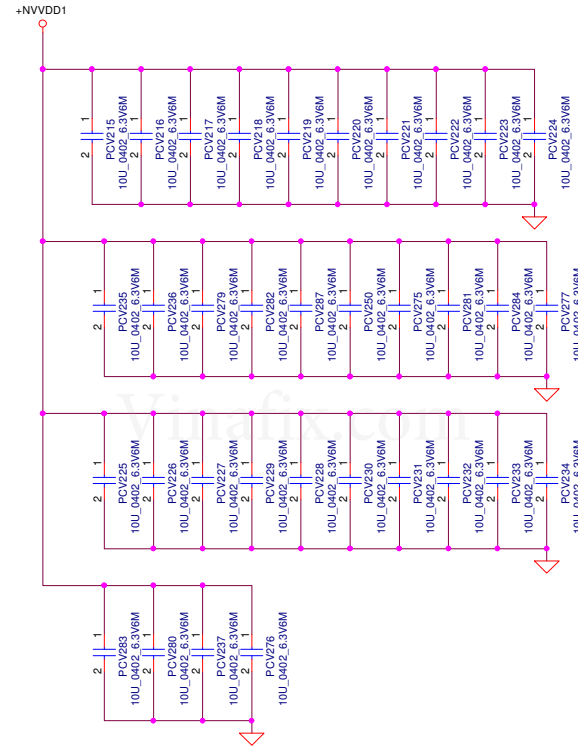
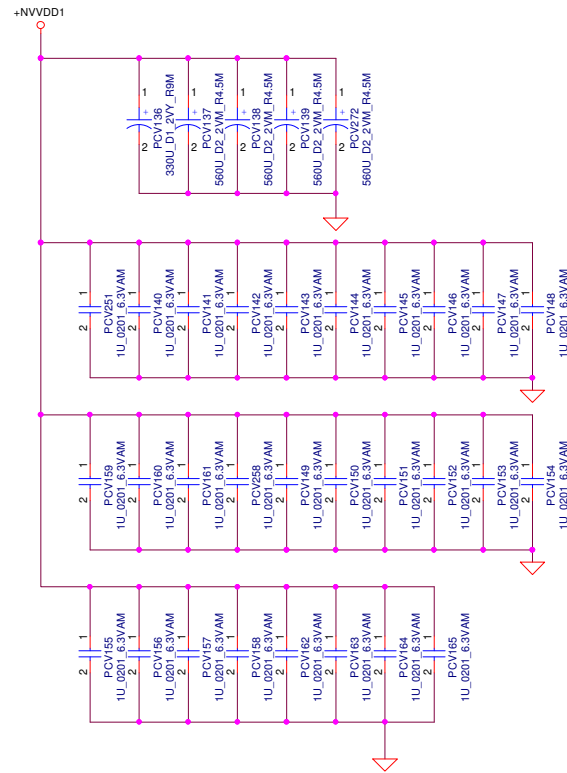
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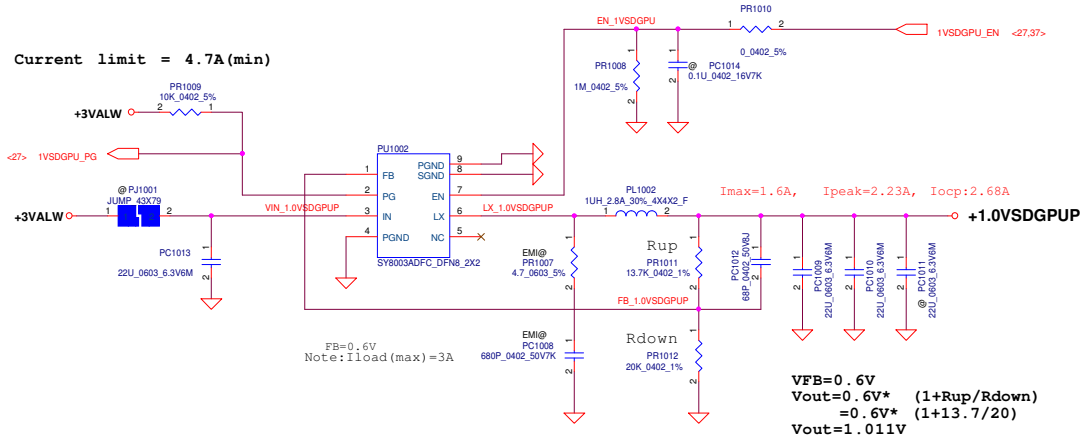
N18P-G0
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402 X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side) ¹		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

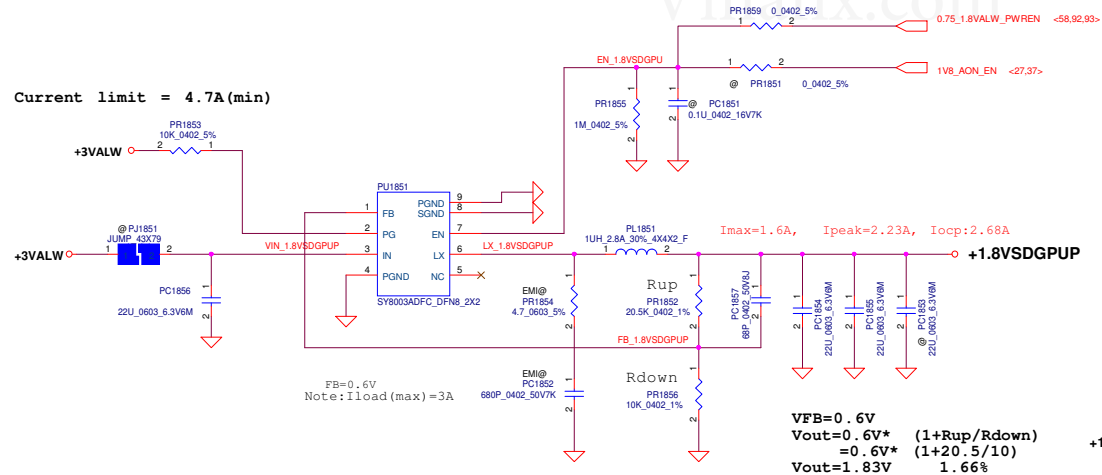


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Choke 1uH SH00000YG00 (Common Part)
(Size:3.8 x 3.8 x 1.9 mm)
Isat:3.42A
(DCR:20m~25m)
Choke: SH00000YG00 Size:4x4x2 (Common Part)
Rdc=27± 20% Taiyo
Rdc=20mohm(Typ), 25mohm(Max) Cyntec
Rdc=27± 20% 3L
Rdc=30± 20% Tai-Tech
Rdc=32± 20% Chillisin
Rdc=36mohm(Typ), Xmohm(Max) Maglayers



Choke 1uH SH00000YG00 (Common Part)
(Size:3.8 x 3.8 x 1.9 mm)
Isat:3.42A
(DCR:20m~25m)
Choke: SH00000YG00 Size:4x4x2 (Common Part)
Rdc=27± 20% Taiyo
Rdc=20mohm(Typ), 25mohm(Max) Cyntec
Rdc=27± 20% 3L
Rdc=30± 20% Tai-Tech
Rdc=32± 20% Chillisin
Rdc=36mohm(Typ), Xmohm(Max) Maglayers



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01	Design Update	DOWN SIZE	0.1		PCB10,PC301,PC501,PCF2_SE042104K80_to_SE00000W210_0.1U_0603_25V7K ->0.1U_0402_25V7K PL101_SM01000U600_to_unpop	2020/03/06	A
02	Design Update	EMI request avoid B2B mos burn ESD request reduce part count	0.1		Add PCB29_NA_to_SE00000X200_10u_0603_25V Add PCB30_NA_to_SE074681K80_680p_0402_50V PRB37-->PHB37_SD028000080_to_SL200003200_0_0402_5%-->10K_0402_50%_TPM0S103P130R PRB13_SD034665280_to_SD034681280_66.5K_0402_1%-->68.1K_0402_1% PRM5_SD034619180_to_SD034634180_6.19K_0402_1%-->6.34K_0402_1% PRB17,PRB14,PRB25,PRZ43,PRZ45,PRZ47,PRV20,PRV34,PRV18,PRV16,PRV145,PRV146,PRV54,PRV56,PRV50,PRV70,PRV51,PRV82, PRV85,PRV79,PRV84,PRV81,PRV92,PRV95,PRV89,PRV94,PRV91,PRW9,PRW26,PRW20 _SD028000080_to_SD028000080_0_0402_5%-->RSHORT PRB16_SD013000080_to_SD013000080_0_0603_5%-->RSHORT	2020/03/13	A
03	Design Update	EMI request	0.1		PC101_SE071101J80_to_SE074102K80_100P_0402_50V8J->1000P_0402_50V7K PRZ24,PRZ40,PRZ45_NA_to_SD001470B80_unpop->4.7_1206_5% PCZ26,PCZ43,PCA11,PCZ49_NA_to_SE074681K80_unpop->680P_0402_50V7K PR18S1_SD028000080_to_NA_0_0402_5%-->unpop	2020/03/18	A
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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HW Schematic chang list (P.I.R)

[illegible]